

# LV530 KBL/ SKL Schematics

## Kabylake-U

### U22 / U2+3e / U42

#### RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance  
For the value, it can be read by the number before R. (R means resistor)  
For the tolerance, it can be read from the last letter.  
For the rating, we don't show on the symbol name.  
For the size, R2=>0402, R3=>0603, R5=>0805,....

#### CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is  
Capacitor type + value + rating + size + tolerance + material  
SCD1U10V2MX-1  
SC=> SMT Ceramic, TC=> POS cap or SP cap  
D1U => 0.1uF  
10V => the voltage rating is 10V  
2=> 0402, 3=>0603, 5=>0805  
M=>tolerance M, K, Z  
X=> X7R/X5R, Y=> Y5V  
1 => symbol version, nonsense to EE characteristic

DY	DUMMY
DY-EMC	Follow EMC team request (SDV DY)
EMC-TVS	SDV : ASM FVT&SIT : By SKU (SKU1 DY / SKU2 ASM)
EMC-TEST	For EMC team SDV test (SDV : ASM)
23e	U2+3e only
U42	U42 only
NON-U42	U22 or U2+3e
UMA	UMA only
PX	Discrete only

<Variant Name>

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Wistron Corporation

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Title

COVER PAGE

Size A3

Document Number

Rev

Date: Friday, December 15, 2017

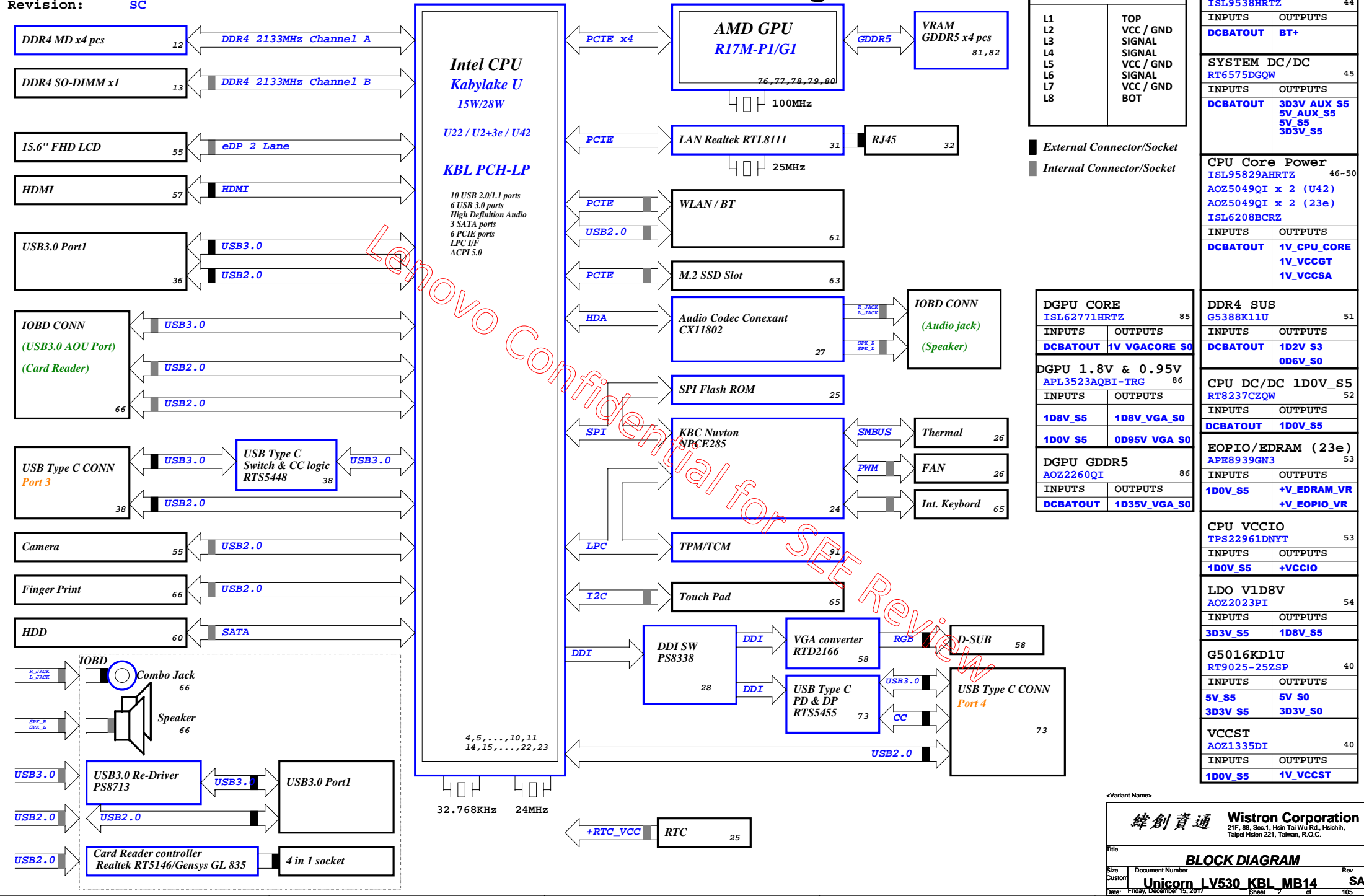
Unicorn LV530 KBL MB14

SA

Sheet 1

of 105

# LV315 KBL-U Block Diagram



PCB LAYER	
L1	TOP
L2	VCC / GND
L3	SIGNAL
L4	SIGNAL
L5	VCC / GND
L6	SIGNAL
L7	VCC / GND
L8	BOT

External Connector/Socket  
Internal Connector/Socket

CHARGER	
ISL9538HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT6575DGQW 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX S5 5V_AUX S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95829AHRTZ 46~50 AOZ5049QI x 2 (U42) AOZ5049QI x 2 (23e) ISL6208BCRZ	
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE 1V_VCCGT 1V_VCCSA
DDR4 SUS	
G5388K11U 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0
CPU DC/DC 1D0V_S5	
RT8237CZQW 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
EOPIO/EDRAM (23e)	
APE8939GN3 53	
INPUTS	OUTPUTS
1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR
CPU VCCIO	
TPS22961DNYT 53	
INPUTS	OUTPUTS
1D0V_S5	+VCCIO
LDO V1D8V	
AOZ2023PI 54	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
G5016KD1U	
RT9025-25ZSP 40	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
VCCST	
AOZ1335DI 40	
INPUTS	OUTPUTS
1D0V_S5	1V_VCCST

DGPU CORE	
ISL62771HRTZ 85	
INPUTS	OUTPUTS
DCBATOUT	1V_VGACORE S0
DGPU 1.8V & 0.95V	
APL3523AQBI-TRG 86	
INPUTS	OUTPUTS
1D8V_S5	1D8V_VGA_S0
1D0V_S5	0D95V_VGA_S0
DGPU GDDR5	
AOZ2260QI 86	
INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

<Variant Name>

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BLOCK DIAGRAM	
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Custom	Unicorn LV530 KBL_MB14
Date: Friday, December 15, 2017	Rev SA

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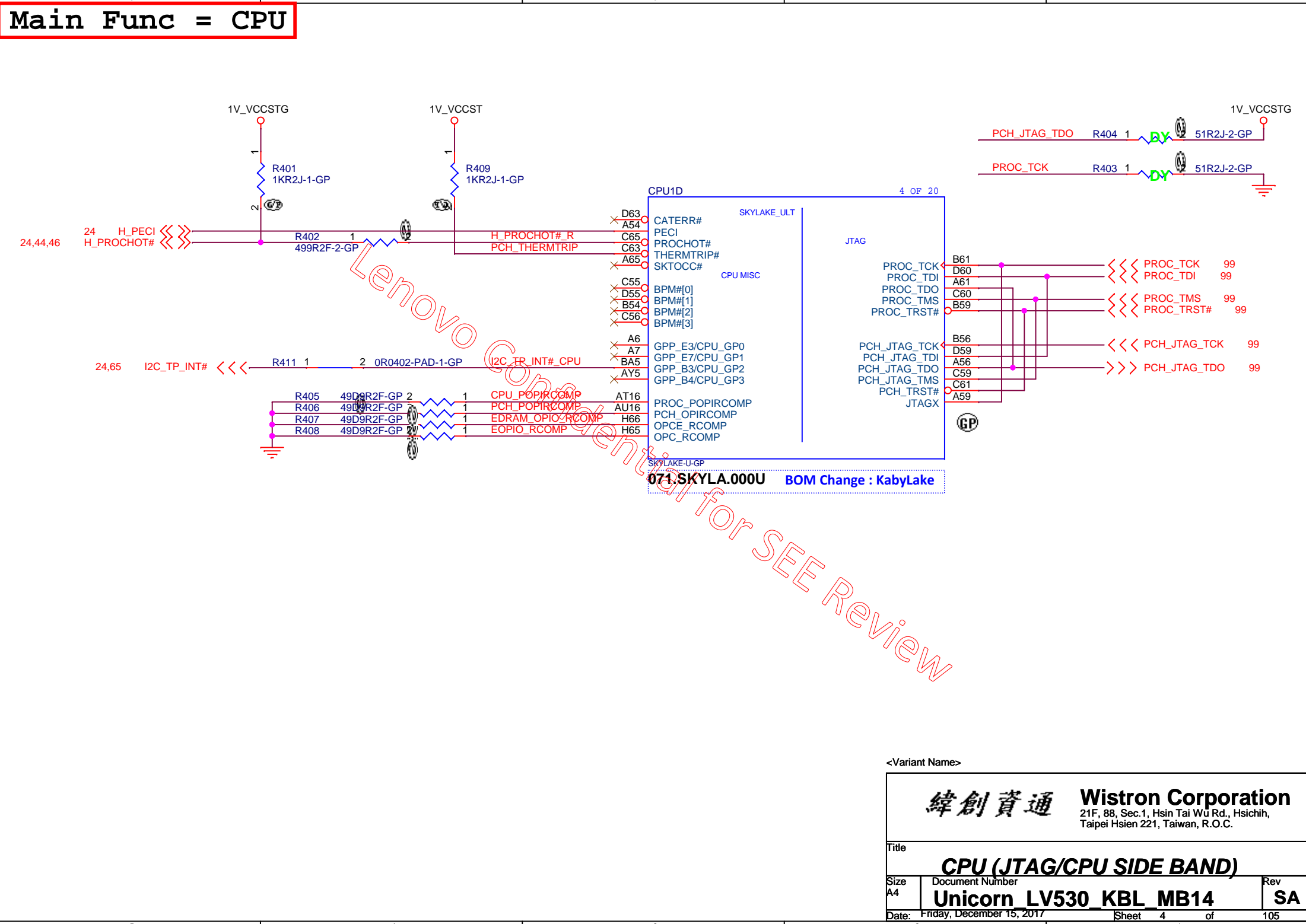
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Size	Document Number		Rev
A4	Unicorn LV530 KBL MB		1A
Date: Friday, December 15, 2017		Sheet 3	of 105

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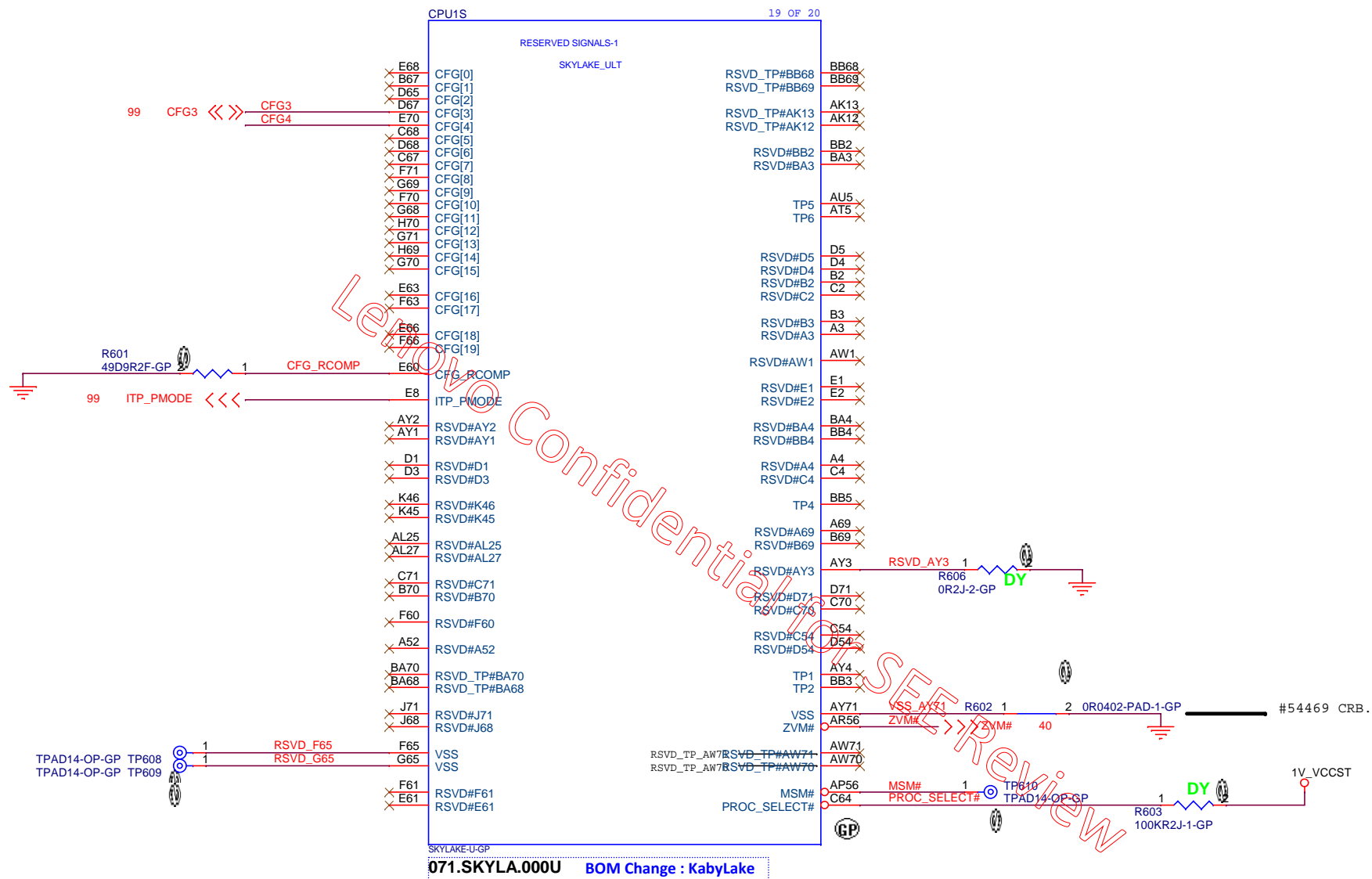


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Title		
CPU (JTAG/CPU SIDE BAND)		
Size	Document Number	Rev
A4	Unicorn LV530_KBL_MB14	SA
Date:	Friday, December 15, 2017	Sheet 4 of 105



## Main Func = CPU



071.SKYLA.000U BOM Change : KabyLake

```
[559100]
CFG[3]: Reserved configuration lane.
CFG[4]: eDP enable:
    1 = Disabled.
    0 = Enabled.
```

**<Variant Name>**

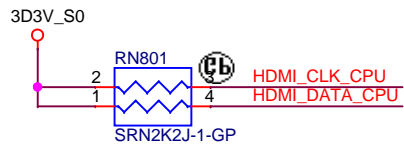
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Title			
CPU (CFG)			
Size	Document Number	Rev	
Custom	Unicorn_LV530_KBL_MB14	SA	
Date:	Friday, December 15, 2017	Sheet	6 of 105





# Main Func = CPU

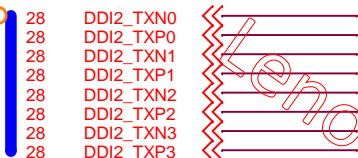


HDMI

20170413

different with BOHO

DDI Switch  
Type C PD, DSUB



HDMI

DDI Switch

+VCCIO

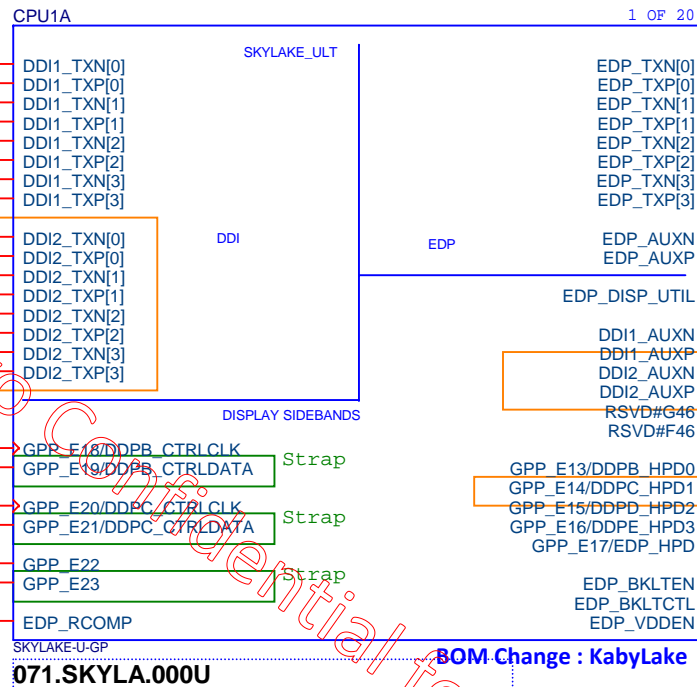


## [561280] eDP\_RCOMP Guideline

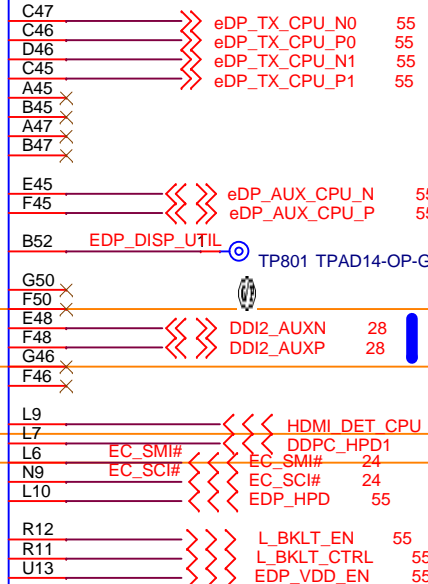
Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 $\Omega$ $\pm$ 1%	Max = 600 mils

## [561280] DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm$ 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm$ 5% resistor	NC

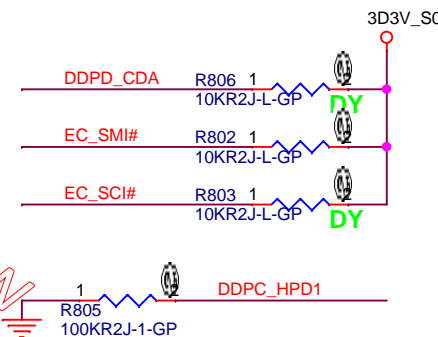


BOM Change : KabyLake



20170413  
different with BOHO

DDI Switch  
Type C PD, DSUB



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Title <b>CPU (DDI/EDP)</b>		
Size A4	Document Number <b>Unicorn LV530_KBL_MB14</b>	Rev <b>SA</b>
Date Friday, December 15, 2017	Sheet 8	of 105



Main Func = CPU

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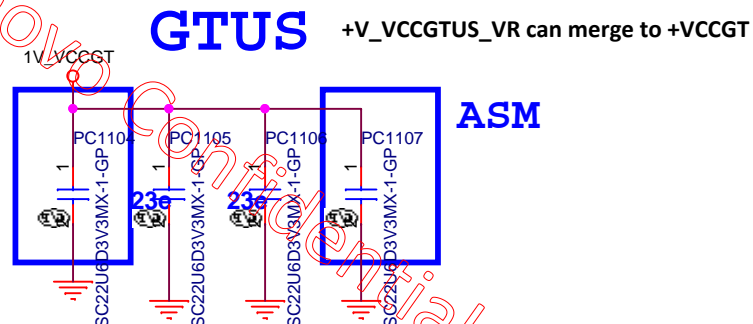
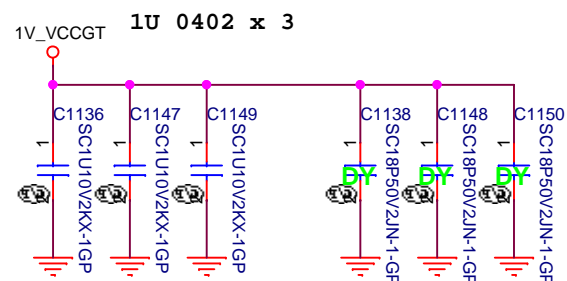
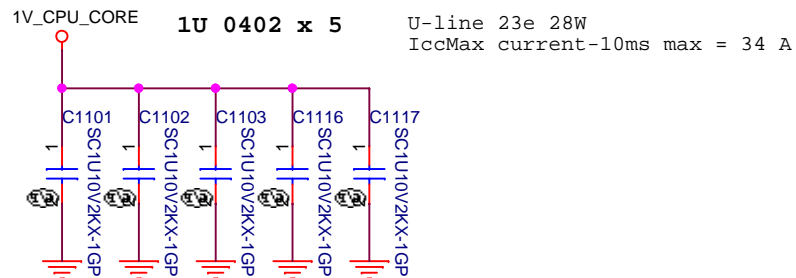
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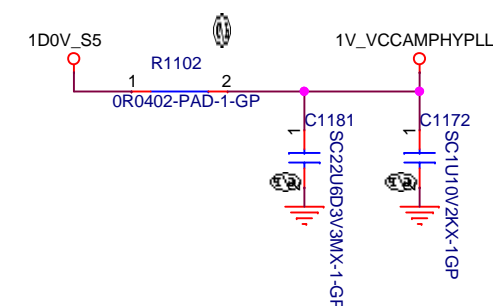
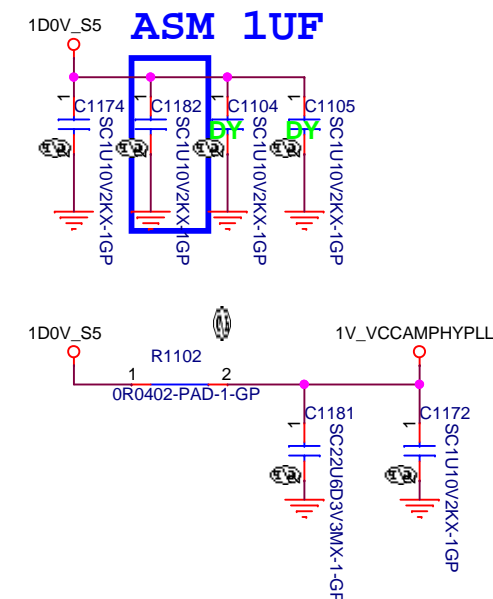
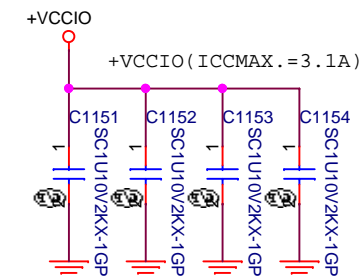
Size A4	Document Number <b>Unicorn LV530 KBL MB 6A</b>	Rev <b>1A</b>
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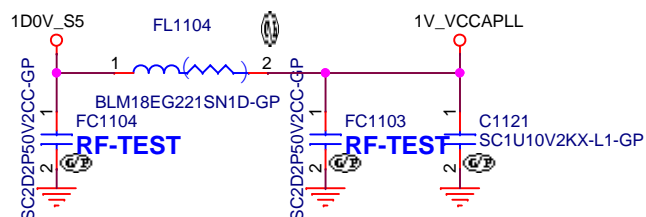
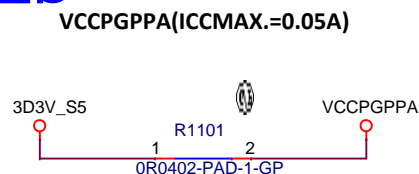
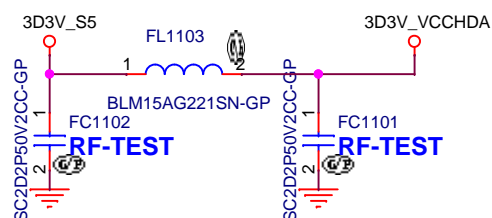
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## VCCIO



## PCH DERIVED RAILS



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Title

CPU (POWER CAP2)

Size  
A4

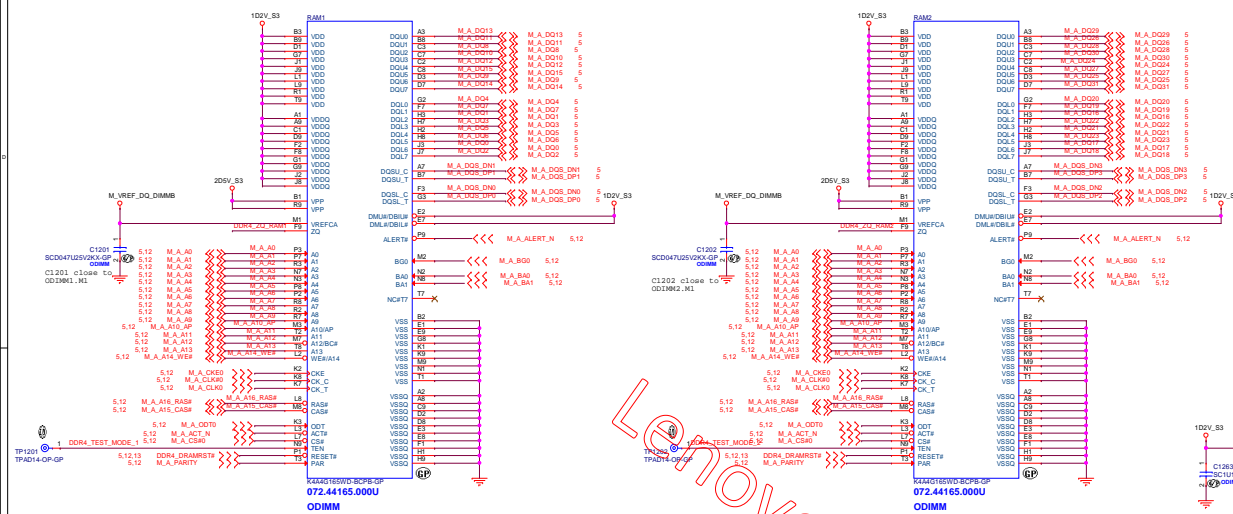
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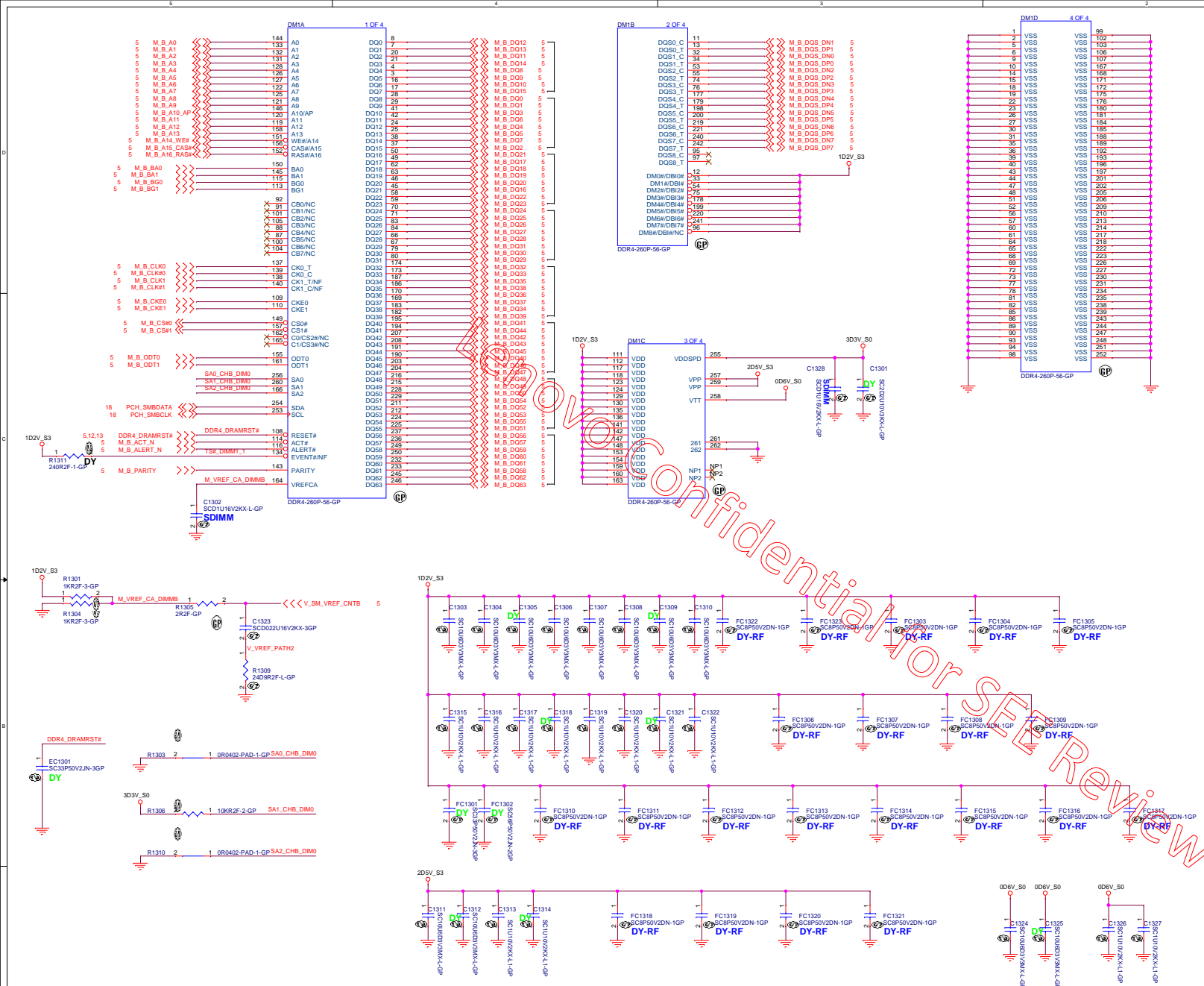
Unicorn\_LV530\_KBL\_MB14

Rev  
SA

Date: Friday, December 15, 2017

Sheet 11 of 105





12/09 Ray  
Need to check property

[561280] 4.23.6 KBL-U DDR4 SODIMM Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 $\mu$ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 $\mu$ F (0402)
	VTT	1 placeholder	1x 330 $\mu$ F (7343)
		Placeholder	1x 10 $\mu$ F (0805)
VPP	DRAM Side	Place these caps on the VTT plane close to SODIMM	1x 10 $\mu$ F (0805)
		Place these caps on the VTT plane close to SODIMM	4x 1 $\mu$ F (0402)
VDDSPD	DRAM Side	Place close to DIMM	2x 10 $\mu$ F (0603)
		Place close to DIMM	2x 1 $\mu$ F (0402)
VDDSPD	DRAM Side	Place close to DIMM	1x 0.1 $\mu$ F (0402)
		Place close to DIMM	1x 2.2 $\mu$ F (0402)

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File			
Size			
Document Number			
Rev			
Unicorn LV530 KBL MB			
Date: Friday, December 15, 2017			
Sheet 13 of 106			

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Title

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Size  
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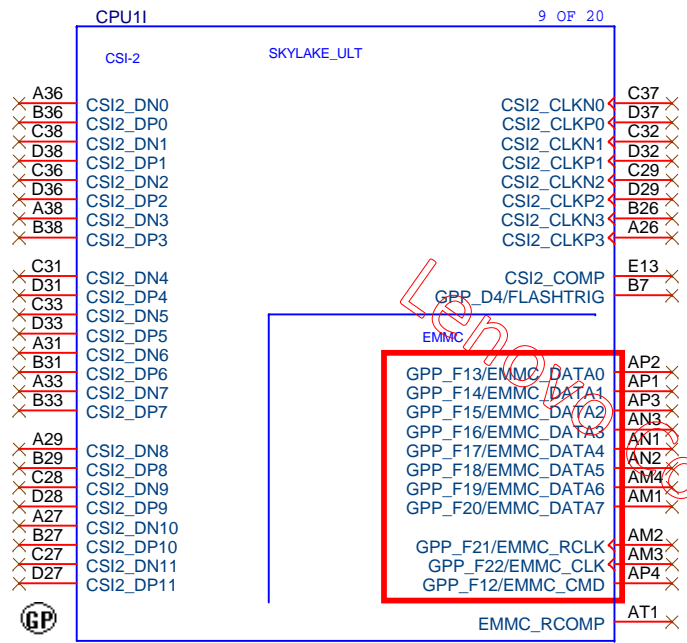
Unicorn LV530 KBL MB 14

Rev

Date: Friday, December 15, 2017

Sheet 14 of 105

Main Func = PCH



SKYLAKE-U-GP  
071.SKYLA.000U BOM Change : KabyLake

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GPP\_F: VCCPGPPF = 1.8V Only

<Variant Name>

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Title <b>CPU (CSI2/EMMC)</b>		
Size A4	Document Number <b>Unicorn LV530 KBL MB 6A</b>	Rev 1
Date: Friday, December 15, 2017 Sheet 15 of 105		



[561280]  
220 nF nominal capacitors are recommended for Gen 3.  
100 nF nominal capacitors are recommended for Gen 2.

GPU 4 x 1

WLAN 1 x 1

LAN 1 x 1

ODD

SATA

HDD

M.2 SSD Optane  
PCIe onlyM.2 SSD Optane  
PCIe / SATA

4 x 1

Share SATA

CPU/H

SPLAKE\_LUT

8 OF 20

[561280] The xHCI controller provides a USB 3.0 debug port capability on all SuperSpeed ports.

USB Port1, Type A USB3.0

USB Port2, Type A USB3.0\_AOU

USB Port3, Type C USB3.0 only

USB Port4, Type C USB3.0, PD, DP

USB Port1, Type A USB2.0

USB Port2, Type A USB2.0\_AOU

USB Port3, Type C USB2.0 only

USB Port4, Type C USB2.0, PD, DP

CAMERA\_USB Port5

CARD READER\_USB Port6

LCD Panel touch\_USB Port7

Bluetooth\_USB Port8

Finger Print\_USB Port9

[561280] Both RCOMP & RCOMPEN need to matched  
less than 1k.83.0005V.CAF  
close to CPU

071SKYLA000U BOM Change : KabyLake

PCIe Table

Port	PCIe Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	M.2 SSD	
6	M.2 SSD	
7	M.2 SSD	SATA0
8	M.2 SSD	SATA1A
9	LAN	
10	WLAN	
11	ODD	SATA1B
12	HDD	SATA2

SATA Table

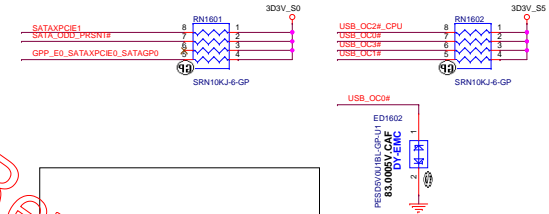
Pair	SATA Device	Share BUS
0	ODD	PCIe7
1A	HDD	PCIe8
1B	M.2 SSD	PCIe11
2	M.2 SSD	PCIe12

USB 3.0 Table

Pair	USB3.0 Device	Share BUS
1	USB3.0 port1 (Type A USB3.0)	
2	USB3.0 Port2 (Type A USB3.0_AOU)	
3	USB Port3, Type C USB3.0 only	
4	USB Port4, Type C USB3.0, PD, DP	
5	N/A	PCIe1 (GPU)
6	N/A	PCIe2 (GPU)

USB 2.0 Table

Pair	USB2.0 Device
1	USB Port1, Type A USB2.0
2	USB Port2, Type A USB2.0_AOU
3	USB Port3, Type C USB2.0 only
4	USB Port4, Type C USB2.0, PD, DP
5	CAMERA_USB Port5
6	CARD READER_USB Port6
7	LCD Panel touch_USB Port7
8	Bluetooth_USB Port8
9	Finger Print_USB Port9
10	Ultrabay USB Port10



&lt;Variant Name&gt;

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File  
Size  
Customer  
Date

Document Number  
Unicorn LV530\_KBL\_MB14

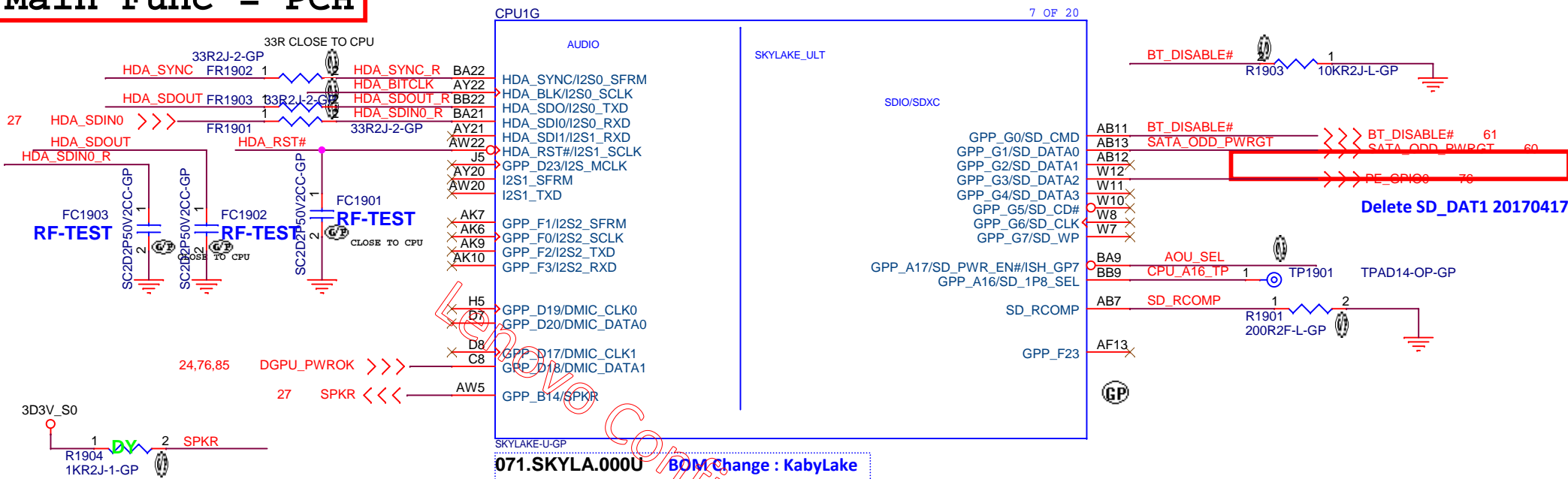
Rev  
SA

Prosy, December 16, 2017 Sheet 16 of 106

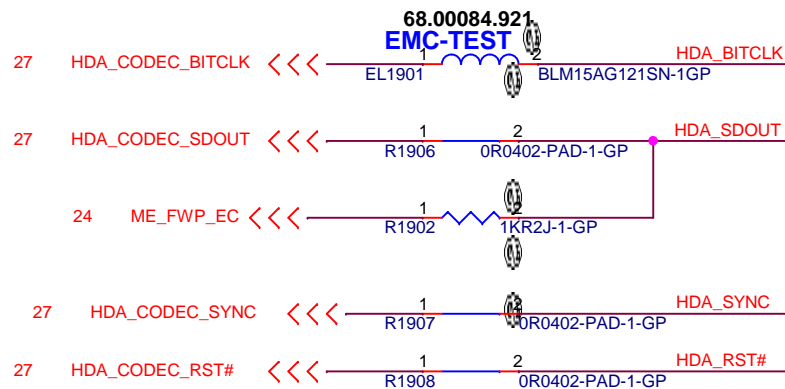


<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.	
file _____			
<b>CPU (LPC/SPI/SMBus/CL/CLK)</b>			
size _____	Document Number _____		
Content _____			
<b>Unicom LV530 KBL MB1 Rev. 1.0</b>			
Date: Friday, December 15, 2017	Printed:	15	of 105

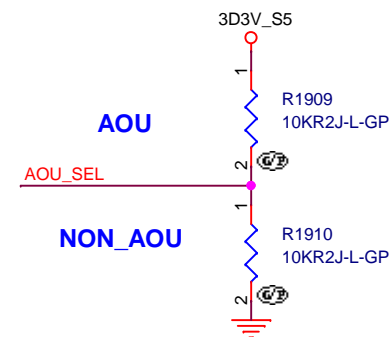
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**SPKR/GPP\_B14**  
Usage: Top Swap Override  
When Sampled: Rising edge of PCH\_PWROK  
The signal has a weak internal Pull-down.  
0 = Disable "Top Swap" mode. (Default)  
1 = Enable "Top Swap" mode.  
The internal Pull-down is disabled after  
PCH\_PWROK de-asserts.  
This signal is in the primary well.



HDA\_SDO\_I2S\_TXD0  
Usage: Flash Descriptor Security Override  
When Sampled: Rising edge of PCH\_PWROK  
The signal has a weak internal Pull-down.  
0 = Enable security measures defined in the Flash Descriptor. (Default)  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.  
The internal Pull-down is disabled after PCH\_PWROK de-asserts.



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Title

### CPU (HDA/SDIO/SDXC)

Size

Document Number

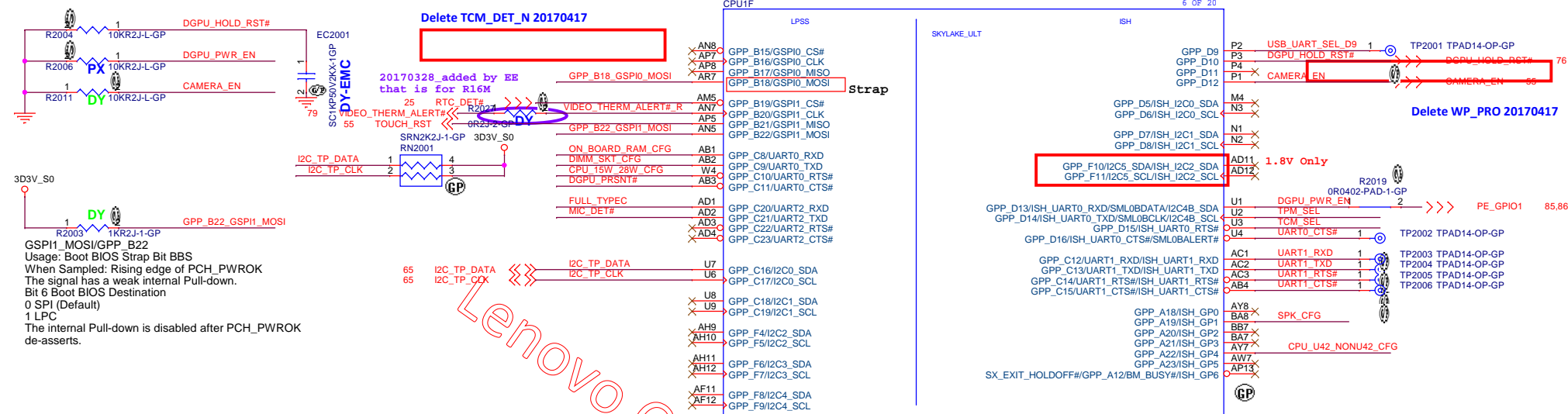
**Unicorn LV530 KBL MB14**

Rev  
**SA**

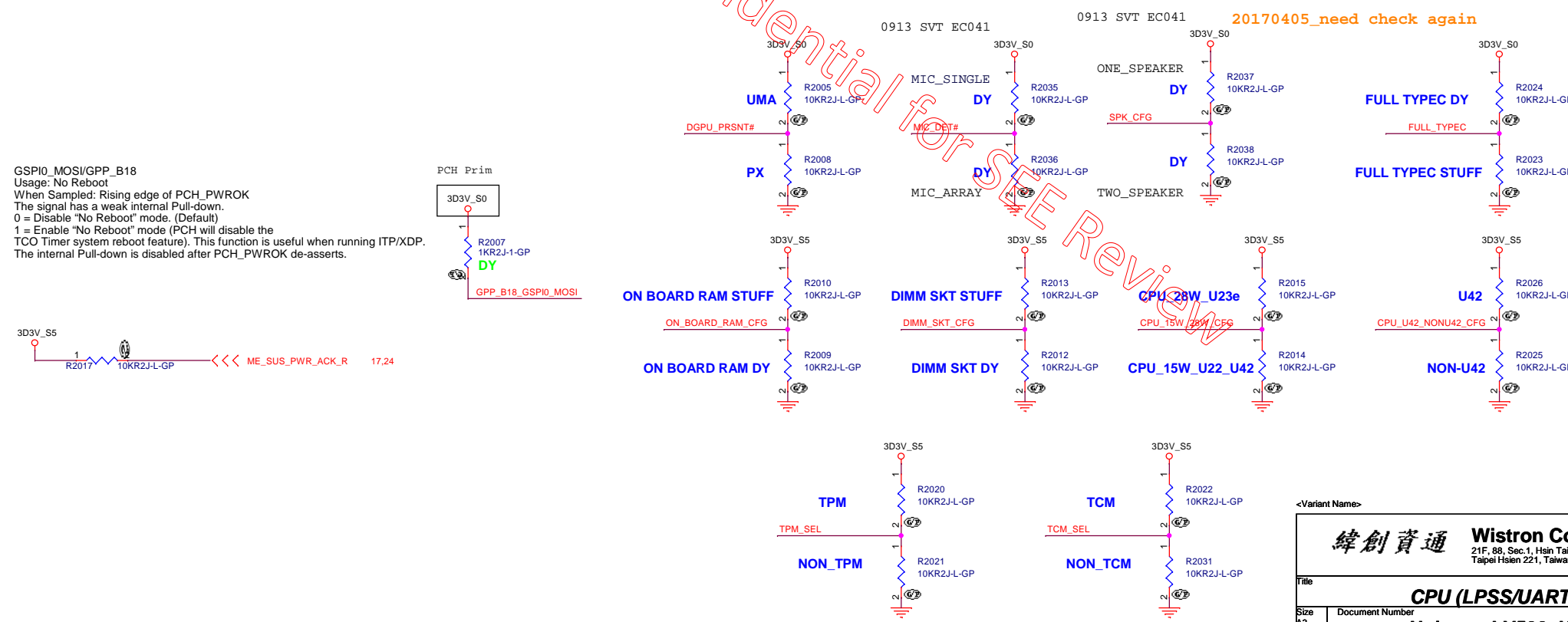
Date: Friday, December 15, 2017

Sheet 19 of 105

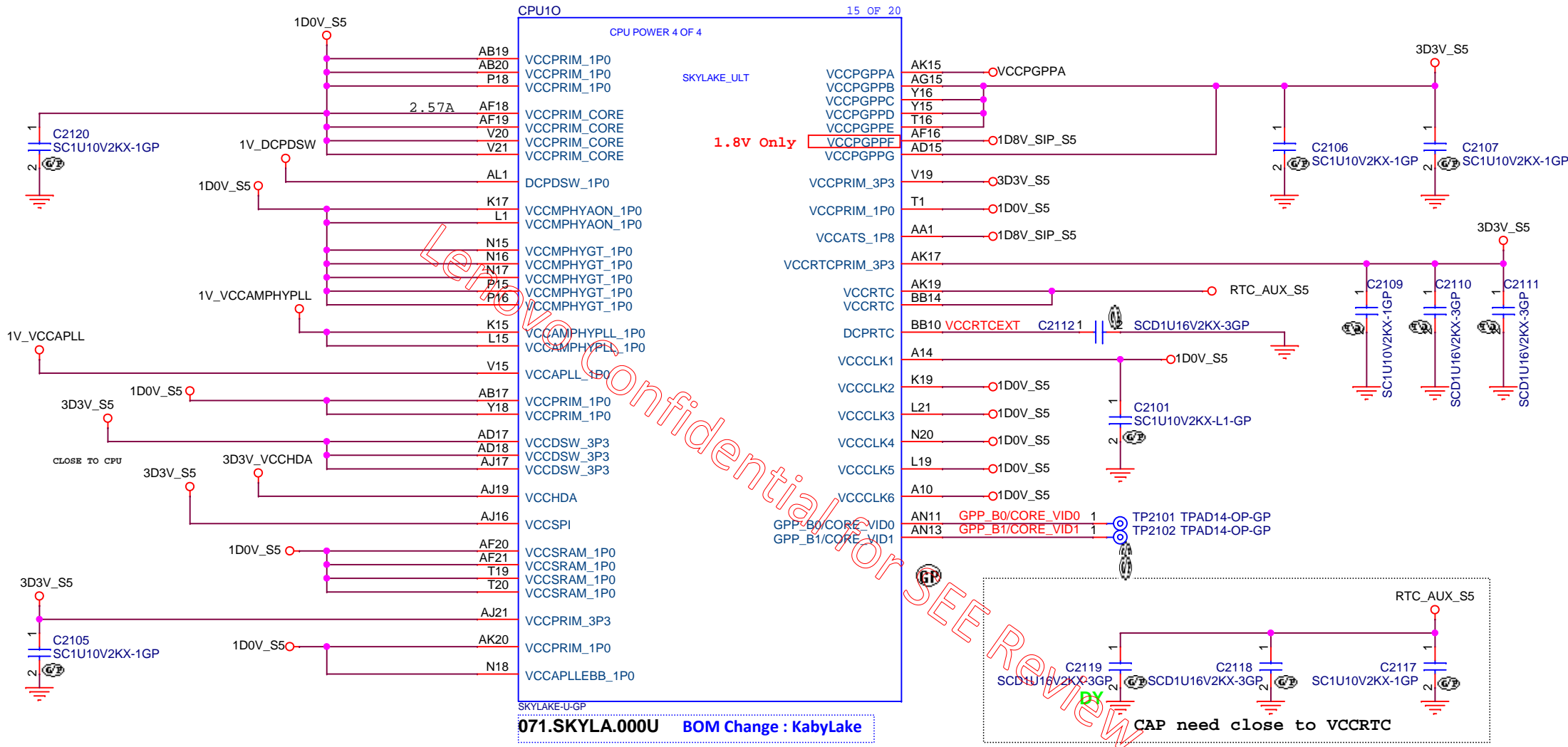
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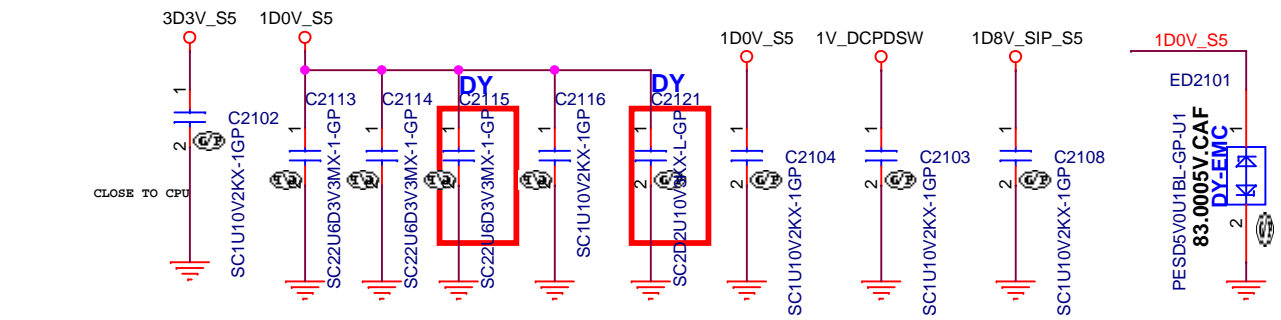
GPIO0\_MOSI/GPP\_B18  
 Usage: No Reboot  
 When Sampled: Rising edge of PCH\_PWROK  
 The signal has a weak internal Pull-down.  
 0 = Disable "No Reboot" mode. (Default)  
 1 = Enable "No Reboot" mode (PCH will disable the  
 TCO Timer system reboot feature). This function is useful when running ITP/XD  
 The internal Pull-down is disabled after PCH\_PWROK de-asserts



Main Func = PCH



071.SKYLA.000U BOM Change : KabyLake



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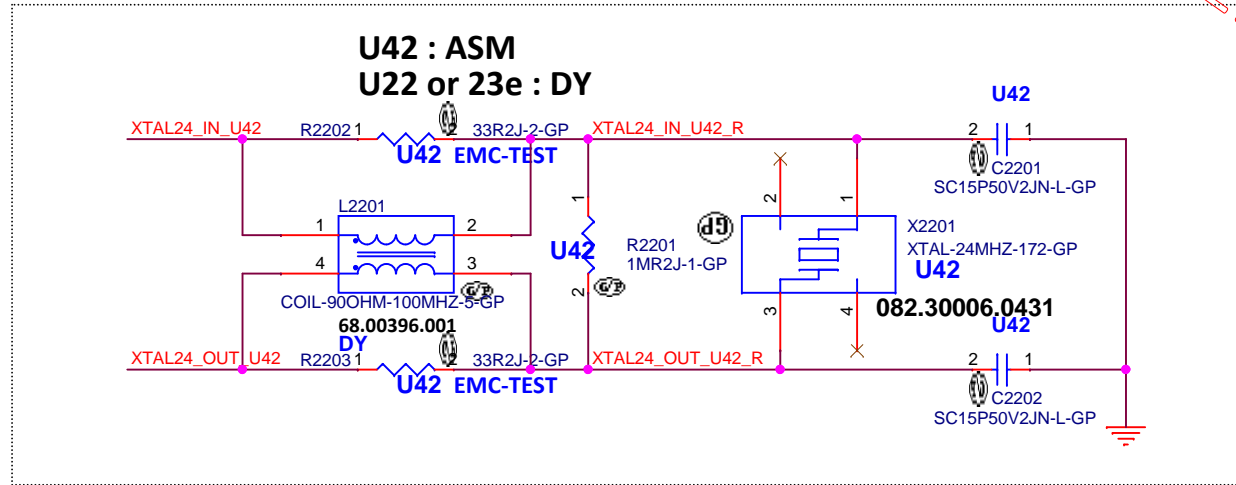
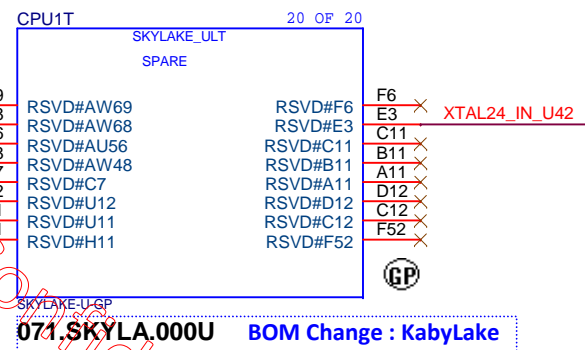
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Size A4	Document Number	Rev
<b>Unicorn LV530 KBL MB</b>		<b>6A</b>

Date: Friday, December 15, 2017 Sheet 21 of 105

Main Func = PCH

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Title			
CPU (RSVD)			
Size	Document Number	Rev	
A4	Unicorn LV530 KBL MB	6A	
Date:	Friday, December 15, 2017	Sheet	22 of 105



Main Func = PCH

CPU1P 16 OF 20

GND 1 OF 3

SKYLAKE\_ULT

A5	VSS	AL65	VSS
A67	VSS	AL66	VSS
A70	VSS	AM13	VSS
AA2	VSS	AM21	VSS
AA4	VSS	AM25	VSS
AA65	VSS	AM27	VSS
AA68	VSS	AM43	VSS
AB15	VSS	AM45	VSS
AB16	VSS	AM46	VSS
AB18	VSS	AM55	VSS
AB21	VSS	AM60	VSS
AB8	VSS	AM61	VSS
AD13	VSS	AM68	VSS
AD16	VSS	AM71	VSS
AD19	VSS	AM8	VSS
AD20	VSS	AN20	VSS
AD21	VSS	AN23	VSS
AD62	VSS	AN28	VSS
AD8	VSS	AN30	VSS
AE64	VSS	AN32	VSS
AE65	VSS	AN33	VSS
AE66	VSS	AN35	VSS
AE67	VSS	AN37	VSS
AE68	VSS	AN38	VSS
AE69	VSS	AN40	VSS
AF1	VSS	AN42	VSS
AF10	VSS	AN58	VSS
AF15	VSS	AN63	VSS
AF17	VSS	AP10	VSS
AF2	VSS	AP18	VSS
AF4	VSS	AP20	VSS
AF63	VSS	AP23	VSS
AG16	VSS	AP28	VSS
AG17	VSS	AP32	VSS
AG18	VSS	AP35	VSS
AG19	VSS	AP38	VSS
AG20	VSS	AP42	VSS
AG21	VSS	AP58	VSS
AG71	VSS	AP63	VSS
AH13	VSS	AP68	VSS
AH6	VSS	AP70	VSS
AH63	VSS	AR11	VSS
AH64	VSS	AR15	VSS
AH67	VSS	AR16	VSS
AJ15	VSS	AR20	VSS
AJ18	VSS	AR23	VSS
AJ20	VSS	AR28	VSS
AJ4	VSS	AR35	VSS
AK11	VSS	AR42	VSS
AK16	VSS	AR43	VSS
AK18	VSS	AR45	VSS
AK21	VSS	AR46	VSS
AK22	VSS	AR48	VSS
AK27	VSS	AR5	VSS
AK63	VSS	AR50	VSS
AK68	VSS	AR52	VSS
AK69	VSS	AR53	VSS
AK8	VSS	AR55	VSS
AL2	VSS	AR58	VSS
AL28	VSS	AR63	VSS
AL32	VSS	AR8	VSS
AL35	VSS	AT2	VSS
AL38	VSS	AT20	VSS
AL4	VSS	AT23	VSS
AL45	VSS	AT28	VSS
AL48	VSS	AT35	VSS
AL52	VSS	AT4	VSS
AL55	VSS	AT42	VSS
AL58	VSS	AT56	VSS
AL64	VSS	AT58	VSS

SKYLAKE-U-GP

071.SKYLEA.000U BOM Change : KabyLake

CPU1Q 17 OF 20

GND 2 OF 3

SKYLAKE\_ULT

AT63	VSS	BA49	VSS
AT68	VSS	BA53	VSS
AT71	VSS	BA57	VSS
AU10	VSS	BA6	VSS
AU15	VSS	BA62	VSS
AU20	VSS	BA66	VSS
AU32	VSS	BA71	VSS
AU38	VSS	BB18	VSS
AV1	VSS	BB26	VSS
AV68	VSS	BB30	VSS
AV69	VSS	BB34	VSS
AV70	VSS	BB38	VSS
AV71	VSS	BB43	VSS
AW10	VSS	BB55	VSS
AW12	VSS	BB6	VSS
AW14	VSS	BB60	VSS
AW16	VSS	BB64	VSS
AW18	VSS	BB67	VSS
AW21	VSS	BB70	VSS
AW23	VSS	C1	VSS
AW26	VSS	C25	VSS
AW28	VSS	C5	VSS
AW30	VSS	D10	VSS
AW32	VSS	D11	VSS
AW34	VSS	D14	VSS
AW36	VSS	D18	VSS
AW38	VSS	D22	VSS
		D25	VSS
AW41	VSS	D26	VSS
AW43	VSS	D30	VSS
AW45	VSS	D34	VSS
AW47	VSS	D39	VSS
AW49	VSS	D44	VSS
AW51	VSS	D45	VSS
AW53	VSS	D47	VSS
AW55	VSS	D48	VSS
AW57	VSS	D53	VSS
AW6	VSS	D58	VSS
AW60	VSS	D6	VSS
AW62	VSS	D62	VSS
AW64	VSS	D66	VSS
AW66	VSS	D69	VSS
AW8	VSS	E11	VSS
AY66	VSS	E15	VSS
B10	VSS	E18	VSS
B14	VSS	E21	VSS
B18	VSS	E46	VSS
B22	VSS	E50	VSS
B30	VSS	E53	VSS
B34	VSS	E56	VSS
B39	VSS	E6	VSS
B44	VSS	E65	VSS
B48	VSS	E71	VSS
B53	VSS	F1	VSS
B58	VSS	F13	VSS
B62	VSS	F2	VSS
B66	VSS	F22	VSS
B71	VSS	F23	VSS
BA1	VSS	F27	VSS
BA10	VSS	F28	VSS
BA14	VSS	F32	VSS
BA18	VSS	F33	VSS
BA2	VSS	F35	VSS
BA23	VSS	F37	VSS
BA28	VSS	F38	VSS
BA32	VSS	F4	VSS
BA36	VSS	F40	VSS
F68	VSS	F42	VSS
BA45	VSS	BA41	VSS

SKYLAKE-U-GP

071.SKYLEA.000U BOM Change : KabyLake

CPU1R 18 OF 20

GND 3 OF 3

SKYLAKE\_ULT

F8	VSS	L18	VSS
G10	VSS	L2	VSS
G22	VSS	L20	VSS
G43	VSS	L4	VSS
G45	VSS	L8	VSS
G48	VSS	N10	VSS
G5	VSS	N13	VSS
G52	VSS	N19	VSS
G55	VSS	N21	VSS
G58	VSS	N6	VSS
G6	VSS	N65	VSS
G60	VSS	N68	VSS
G63	VSS	P17	VSS
G66	VSS	P19	VSS
H15	VSS	P20	VSS
H18	VSS	P21	VSS
H71	VSS	R13	VSS
J11	VSS	R6	VSS
J13	VSS	T15	VSS
J25	VSS	T17	VSS
J28	VSS	T18	VSS
J32	VSS	T2	VSS
J35	VSS	T21	VSS
J38	VSS	T4	VSS
J42	VSS	U10	VSS
J8	VSS	U63	VSS
K16	VSS	U64	VSS
K18	VSS	U66	VSS
K22	VSS	U67	VSS
K30	VSS	U69	VSS
K61	VSS	U70	VSS
K63	VSS	V16	VSS
K64	VSS	V17	VSS
K65	VSS	V18	VSS
K66	VSS	W13	VSS
K67	VSS	W6	VSS
K68	VSS	W9	VSS
K70	VSS	Y17	VSS
K71	VSS	Y19	VSS
L11	VSS	Y20	VSS
L16	VSS	Y21	VSS
L17	VSS		

SKYLAKE-U-GP

071.SKYLEA.000U BOM Change : KabyLake

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size  
Custom

Document Number

Rev

Unicorn LV530 KBL MB 6A

Date: Friday, December 15, 2017

Sheet 23 of 105

20170707\_need check

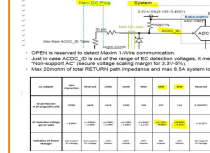
## Model ID BOM Ctrl

PCB VERSION ADP(P98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
ES1_KBL	100.0K	64.10K25.10K	3.0V
ES3_KBL	100.0K	64.20K25.10K	2.75V
V30_KBL	100.0K	33.0K	2.40V
V30_KBL	100.0K	47.0K	2.34V
NA	100.0K	64.9K	2.8V
V10-15KB V10 EC01	100.0K	76.8K	1.87V
NA	100.0K	215.0K	1.048V

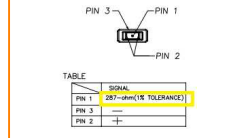
## PCB VERSION

PCB VERSION ADP(P98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
NA	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.40V
SD	100.0K	47.0K	2.34V
-1	100.0K	64.9K	2.8V
-1M	100.0K	76.8K	1.87V
PVT EC01	-2	NA	1.048V
-3	100.0K	133.0K(133.0K ADL)	1.41V
-4	100.0K	174.0K(174.0K ADL)	1.30V

## SPIC: ADP PWR Detection Function V1.3



## DELTA Model:ADP65FD BB-PD03 ADP



## Prevent BIOS data loss solution



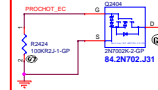
## Nuvoton KBC PSL Power Switched Logic

1. Enter PSL mode (Entry S5 after 10sec) : 3D3V\_AUX\_KBC : OFF (KBC PWR supply)
2. At PSL mode (SPIC: S5<10mV)

EC_ENABLE	S5_ENABLE	3D3V_AUX_KBC
HL	Low	OFF

PSL Wake (AC or DC)	EC_ENABLE	S5_ENABLE	3D3V_AUX_KBC
HL	HL	HL	ON

## EC GPIO47 High Active

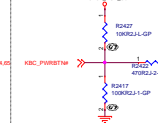


NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.	KBC_NOVO_BTN	ESC_PWRBTN_EC
Low	Low	Low

KBC\_PWRBTN\_EC# : Low  
 (1) 4sec: PWR  
 Button shut down  
 (2) 8sec: KBC reset

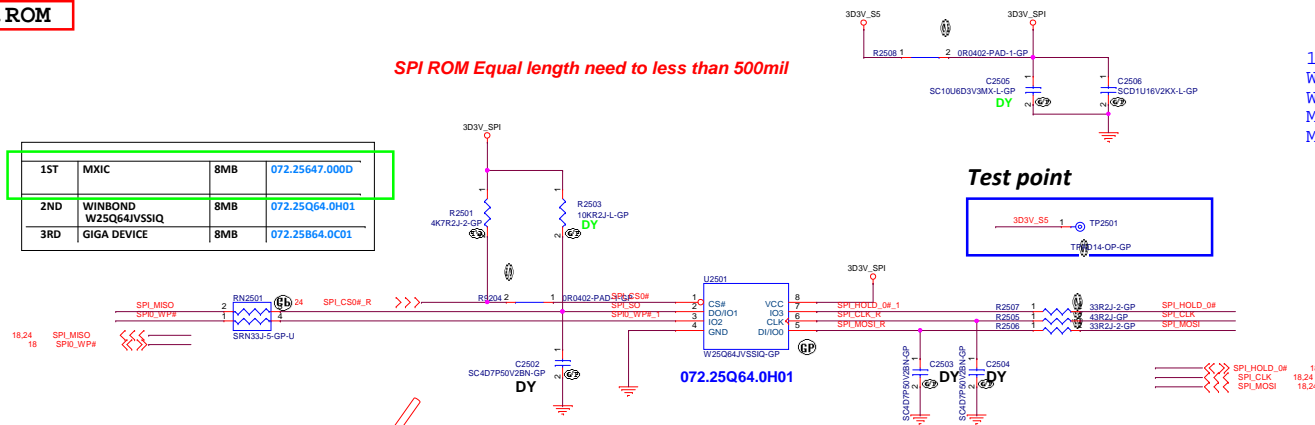
## KBC\_PWRBTN\_EC#



```
SSID = Flash.ROM
```

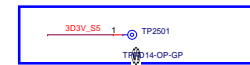
**SPI ROM Equal length need to less than 500mil**

1ST	MXIC	8MB	072.25647.000D
2ND	WINBOND W25Q64JVSSIQ	8MB	072.25Q64.0H01
3RD	GIGA DEVICE	8MB	072.25B64.0C01

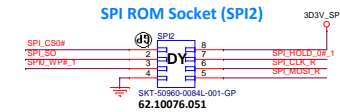


```
16MB SOIC8
WINBOND W25Q128FVSIQ/ 72.25128.0E1
WINBOND W25Q128FVSIQ/ 72.25128.0A1
MACRONIX MX25L12873FM2I-10G/ 72.12873.001
MACRONIX MX25L12873FM2I-10G/ 072.25128.0B11
```

**Test point**

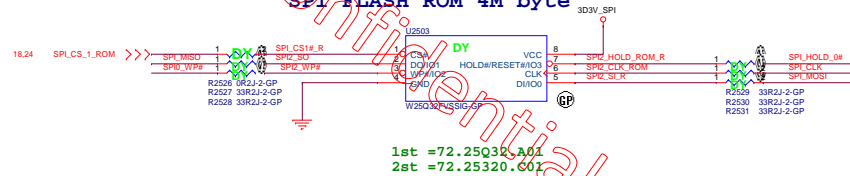


### SPI ROM Socket (SPI2)



### Co-Layout Design on U2501

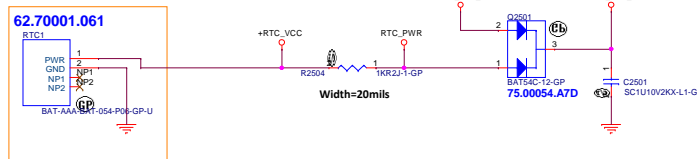
~~SPI~~ FLASH ROM 4M byte



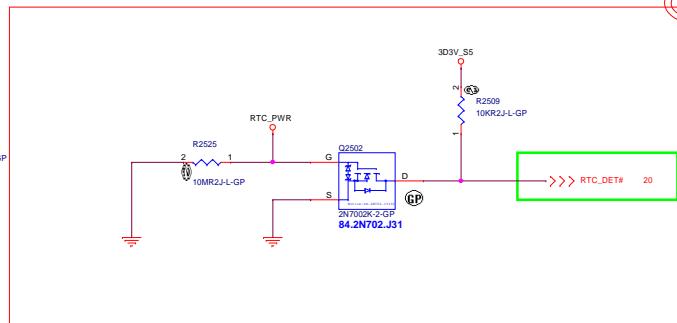
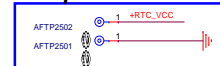
1st = 72.25Q32.A01  
2nd = 72.25320.C01

SSID = RBATT

20170320\_need check pin define  
with ME



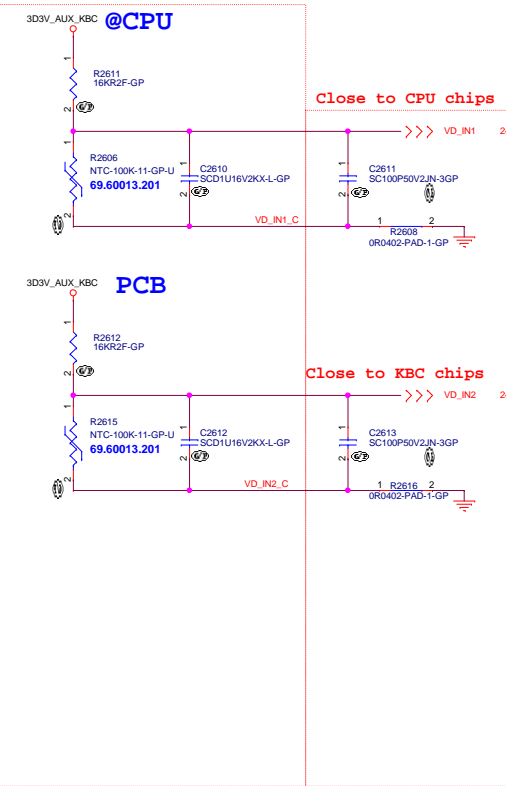
**Test point**



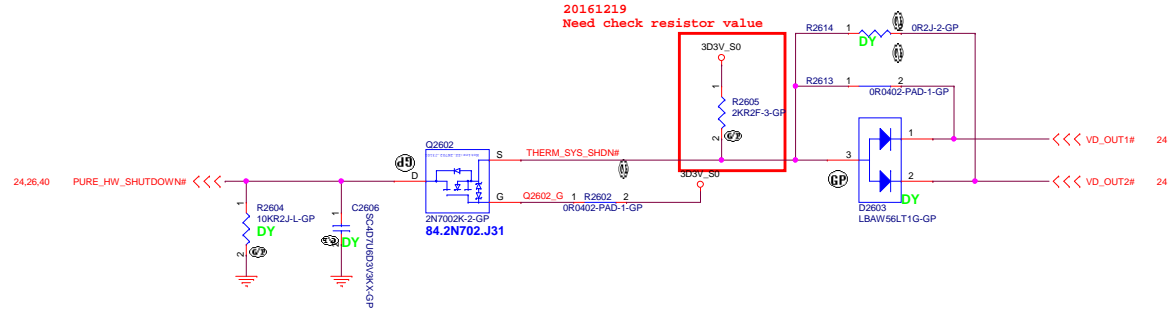
High Detect  
Need to Check whether to PD in PCH Side

Main Func = Thermal Sensor

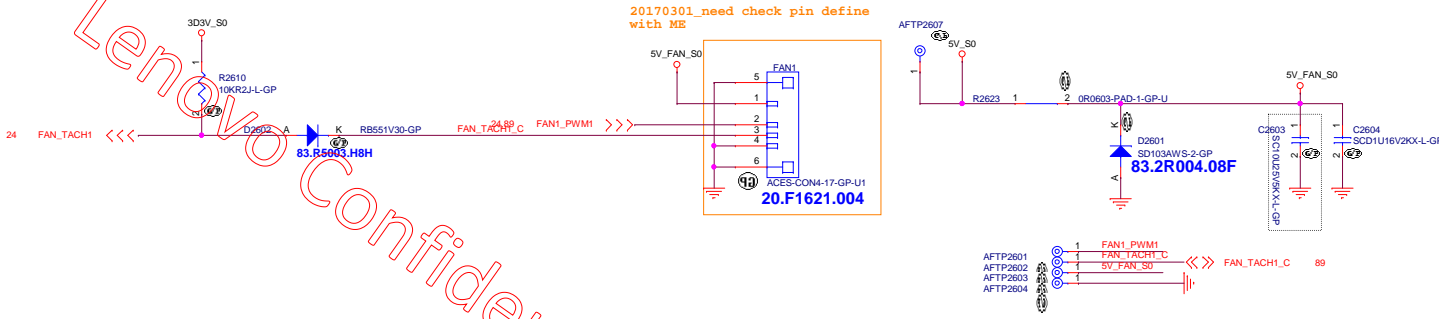
Close to Thermal sensor



20161219  
Need check resistor value

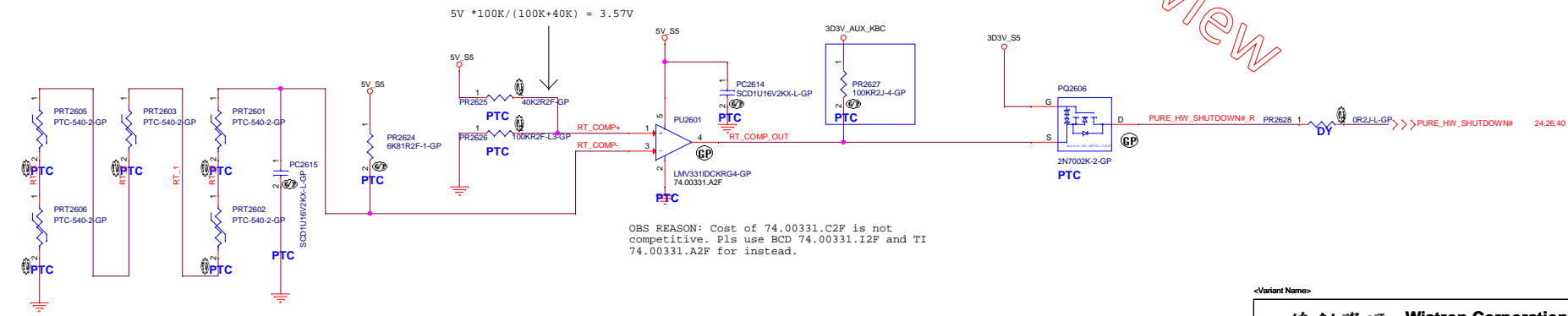


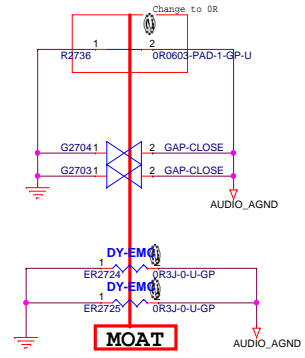
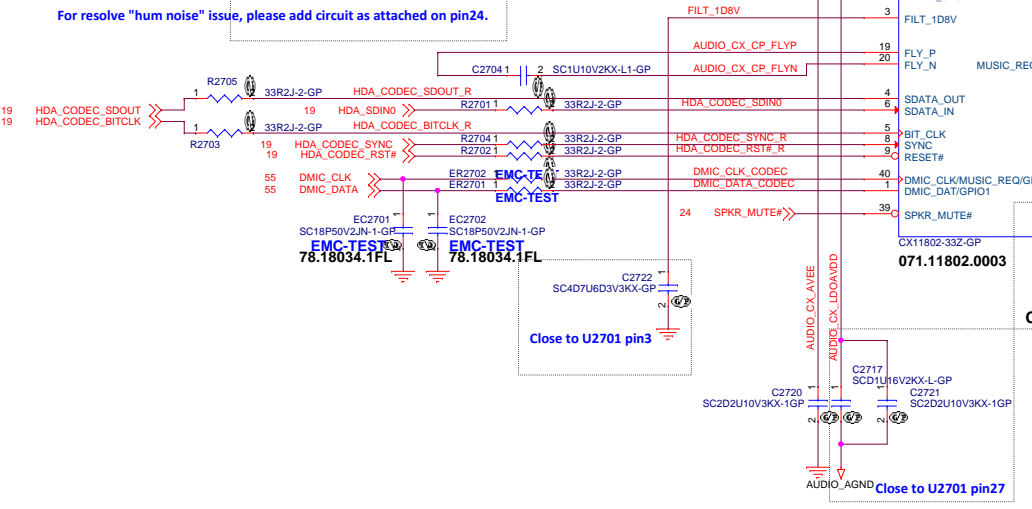
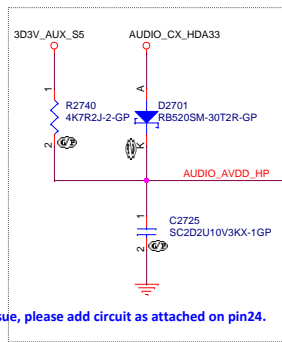
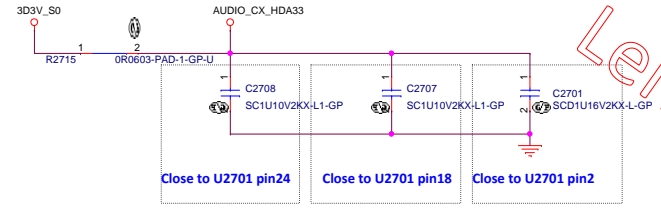
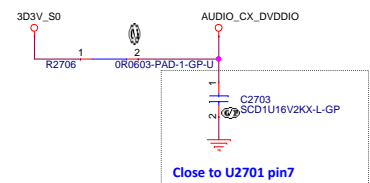
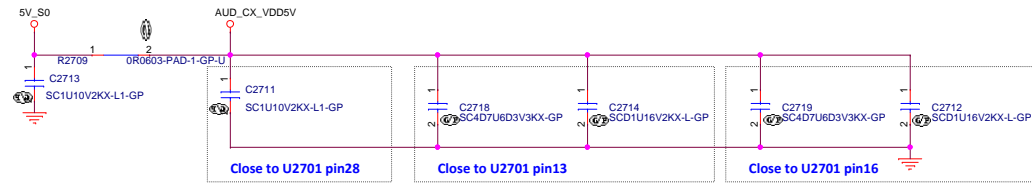
20170301\_need check pin define  
with ME



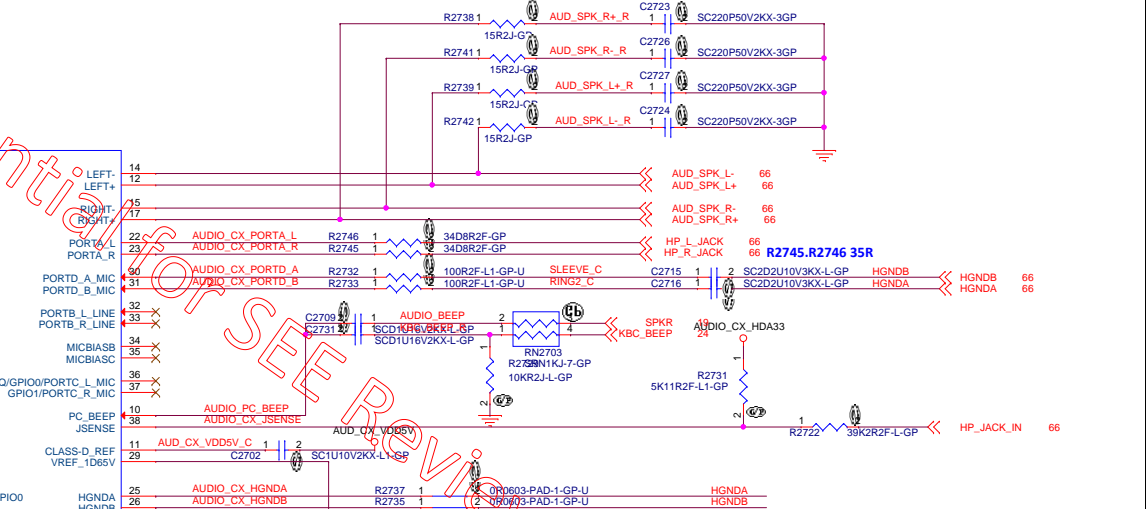
PURE\_HW\_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low





Install snubber networks on each net of SPKs helps control the overshoot/undershoot at the class-D outputs.



Title		Document Number		Rev
AUDIO CODEC CX11802		Unicorn LV530 KBL MB19A		
Date:	Friday, December 15, 2017	Sheet	27	of 105

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI\_PRIORITY2)

L Port 1 has higher priority when both ports are plugged  
H Port 2 has higher priority when both ports are plugged

For Automatic Switching Mode (CFG0 = H):

SW = L: Port1 has higher priority when both ports are plugged (default)

SW = H: Port2 has higher priority when both ports are plugged

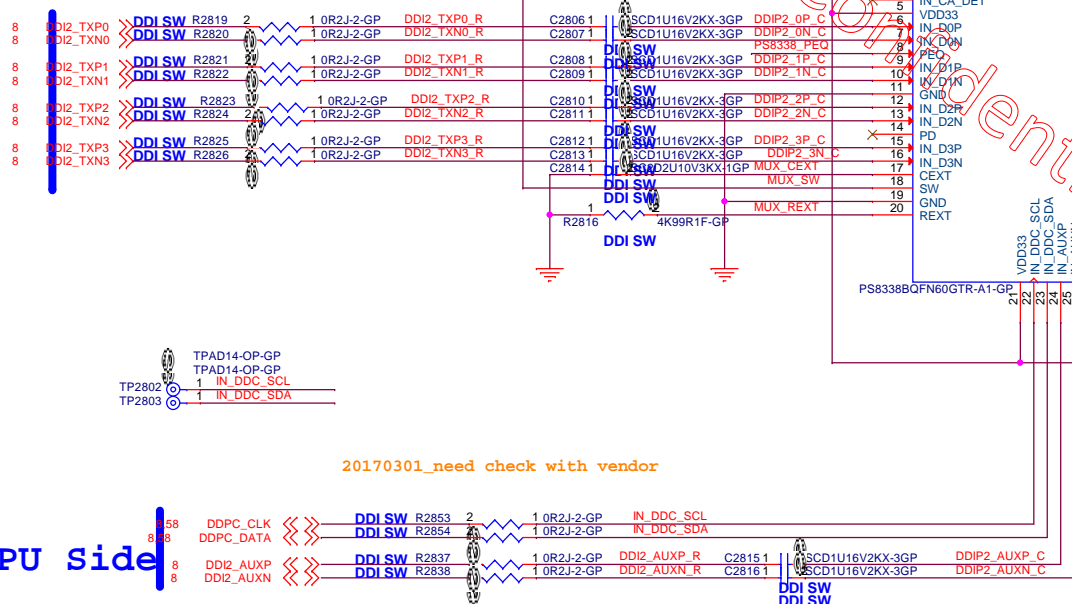
Overwritten by I2C register in I2C Control Mode

Port 2 first

Layout note: extend the length to  
6 inch for DP traces of PS8338B input

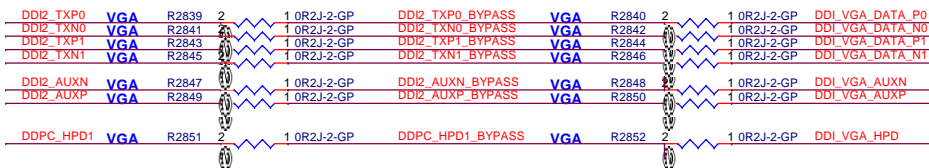
CPU side  
DDI2 IO

TPAD14-OP-GP TP2801



20170301\_need check with vendor

Bypass DDI SW



Closed to  
Type C DP Controller

to VGA DSUB

to Type C DP

20170301\_need check with vendor

to Type C DP

to VGA DSUB

&lt;Variant Name&gt;

緯創資通

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDI Switch

Size

Document Number

Unicorn LV530 KBL MB13A

Date

Friday, December 15, 2017

Sheet

28

of

105

INTERNAL STEREO SPEAKERS

MOVE TO SMALL BOARD

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<Variant Name>			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>AUDIO SPEAKER</b>			
Size	Document Number		Rev
A3	Unicorn_LV530_KBL_MB13A		13A
Date:	Friday, December 15, 2017		Sheet 29 of 105



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<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**(RESERVED)**

Size  
A4

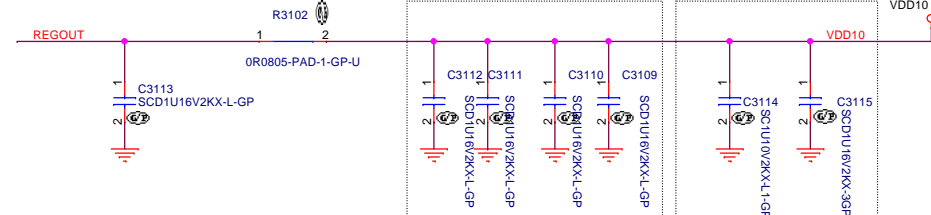
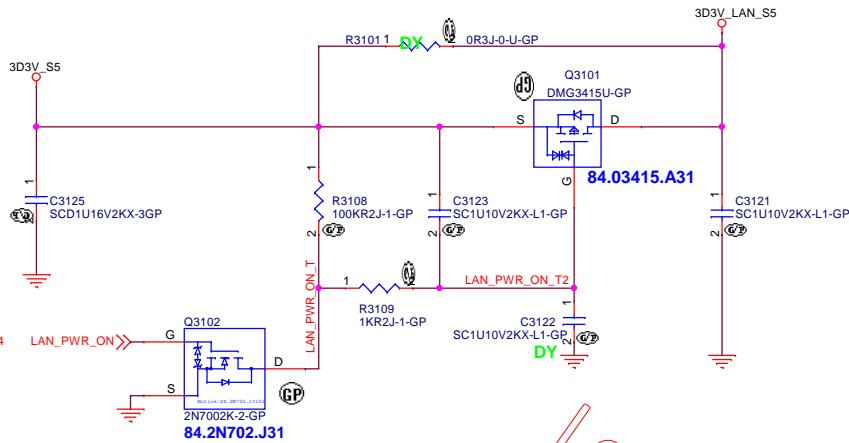
Document Number

**Unicorn\_LV530\_KBL\_MB14BOHOL**

Rev  
SA

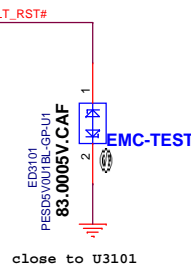
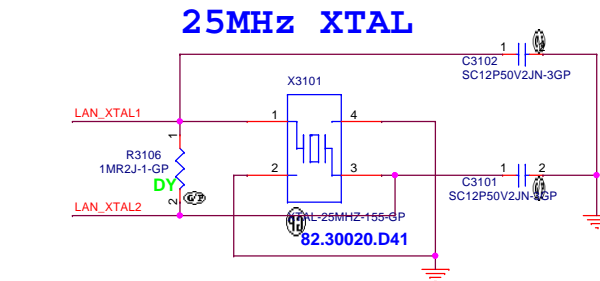
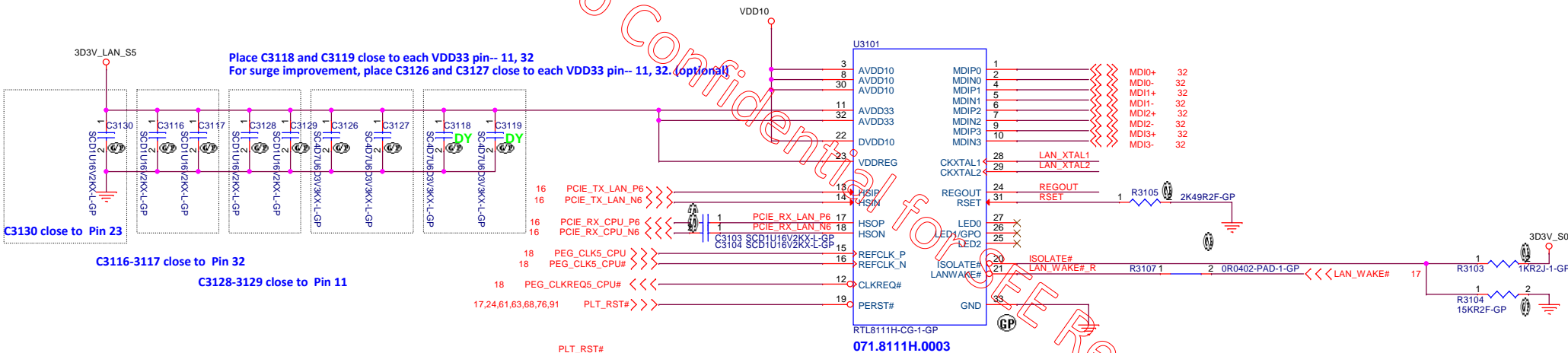
Date: Friday, December 15, 2017

Sheet 30 of 105



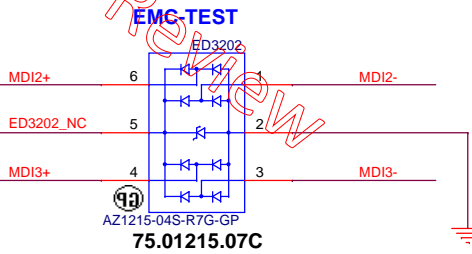
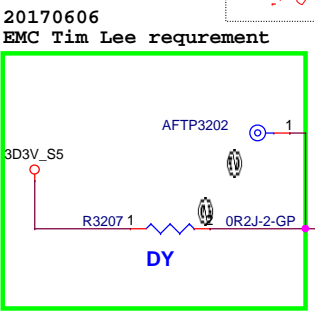
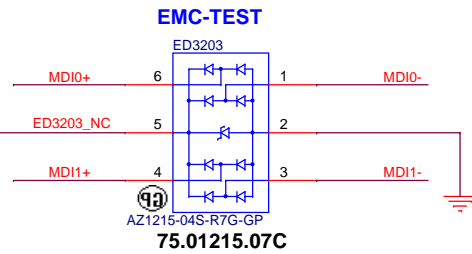
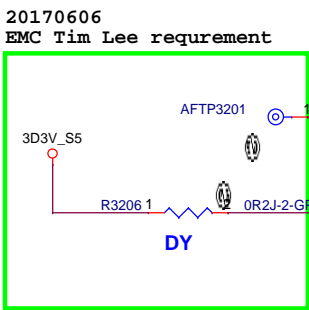
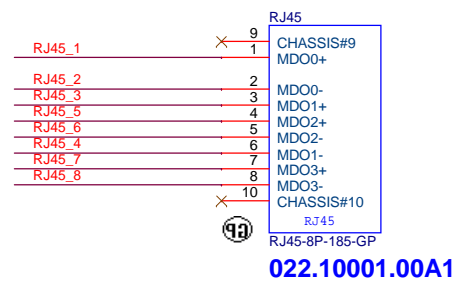
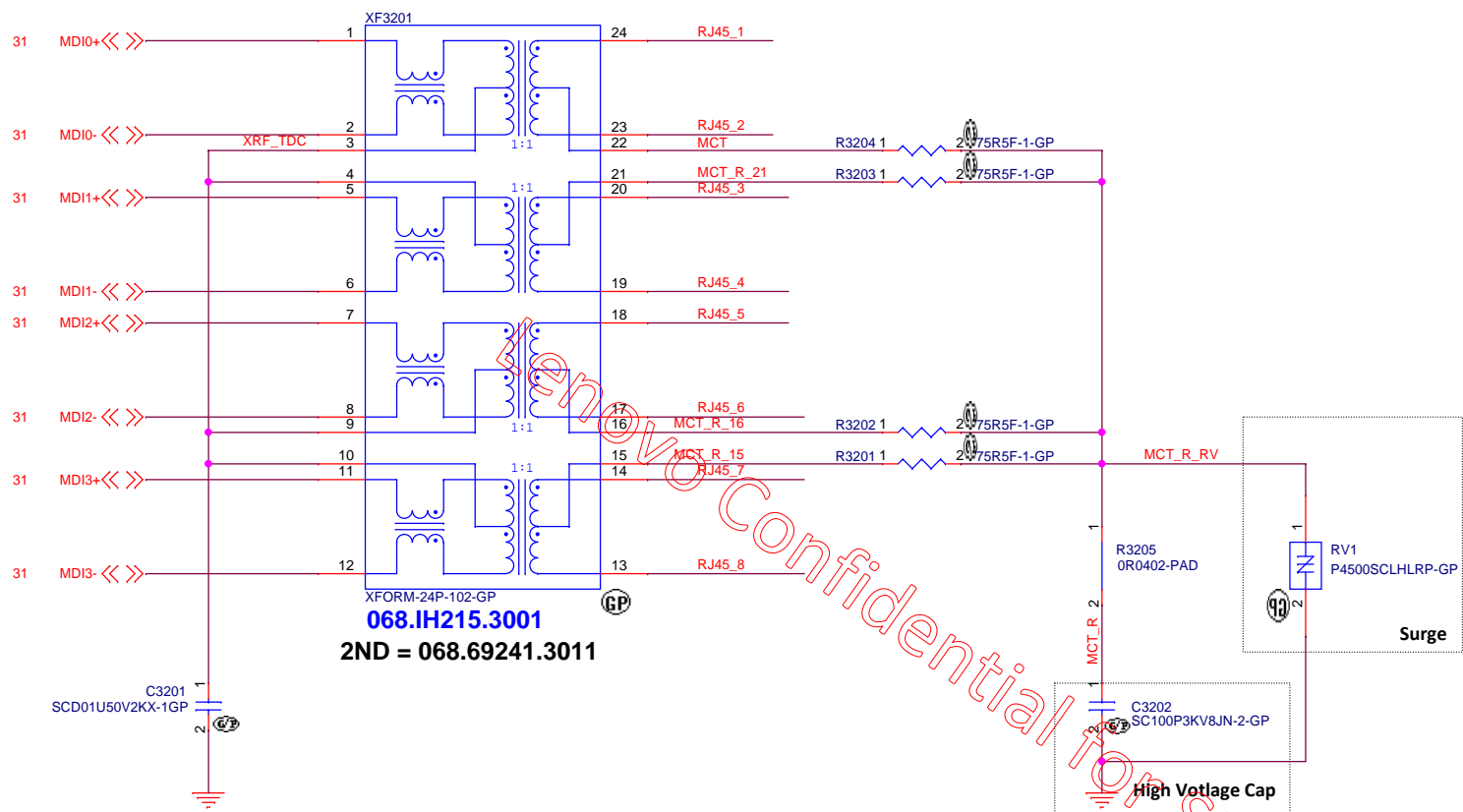
For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS  
\*Place C3109 to C3112 close to each VDD10 pin-- 3, 8, 22, 30

For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS  
\*Place C3114 and C3115 close to each VDD10 pin-- 22 (Reserved)



10/100M/1000M Lan Transformer

LAN Connector



<Variant Name>

Title	
RJ45	
Size	Document Number
Custom	Unicorn LV530 KBL MB13A
Date:	Friday, December 15, 2017
Sheet	32 of 105

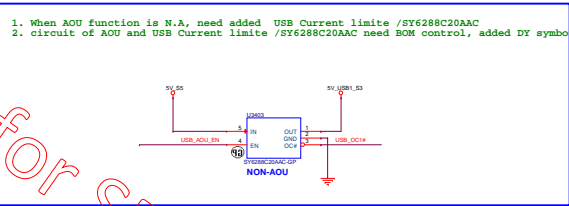
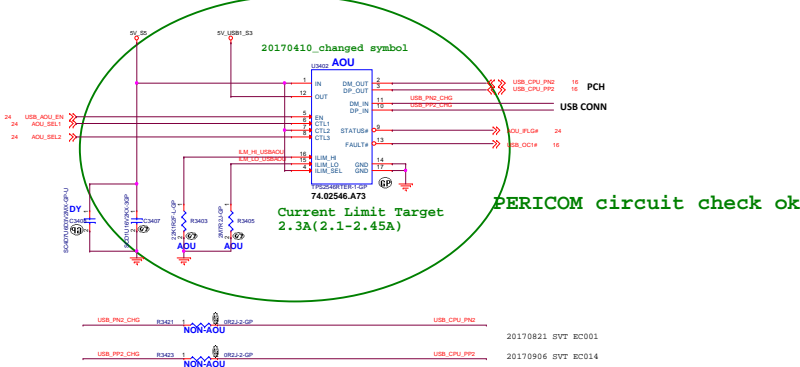
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<Variant Name>

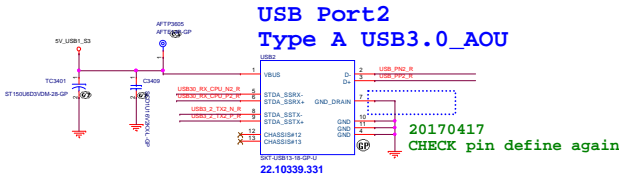
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title (RESERVED)			
Size A3	Document Number Unicorn_LV530_KBL_MB14V530		Rev SA
Date: Friday, December 15, 2017		Sheet 33 of	105

needReserve USB2.0 by pas AOU

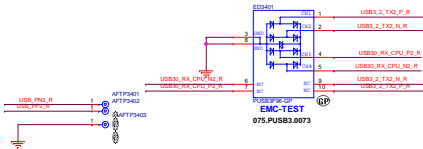
AOU  
1ST,  
TI, 74.02546.A73  
IC PWR SW TPS2546RTER QFN 16P(REV 1.1)  
2ND  
PERICOM, 074.52546.0A73  
IC PWR SW PI5USB2546ZHEX TQFN 16P REV.X



USB Port2  
Type A USB3.0\_AOU



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GNND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GNND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX



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RESERVED

<Variant Name>			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB30 RE-DRIVER			
Size	Document Number		Rev
A3	Unicorn_LV530_KBL_MB13A		13A
Date: Friday, December 15, 2017		Sheet 35 of	105

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<Variant Name>		
<div>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipin Hsien 221, Taiwan, R.O.C.</div>		
Title (RESERVED)		
Size A2	Document Number Unicorn LV530 KBL MB 6A	Rev 6A
Date: Friday, December 15, 2017		
Sheet 95 of 105		

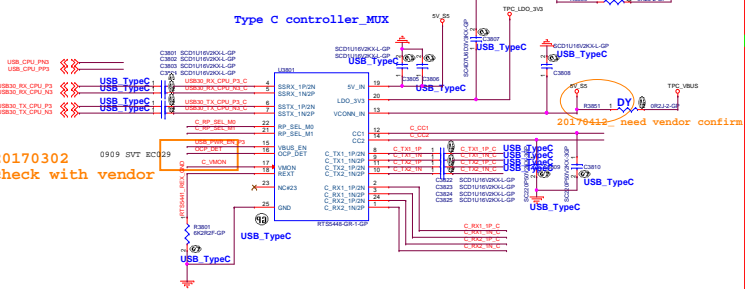


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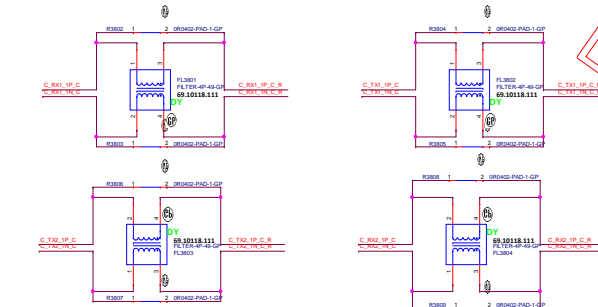
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TYPEC USB3.1-1			
Size	Document Number		Rev
A4	Unicorn LV530 KBL MB SA		1A
Date:	Friday, December 15, 2017		Sheet 37 of 105

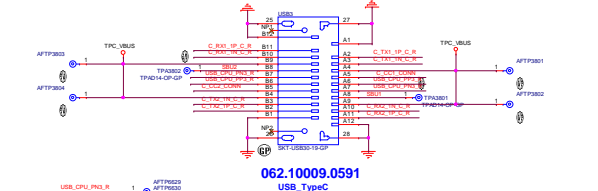
# USB Port3, Type C USB3.0 only



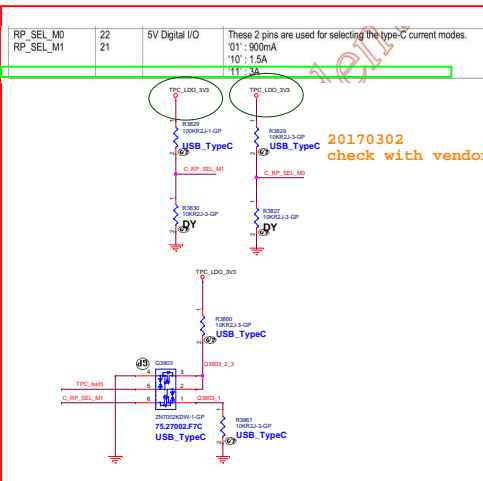
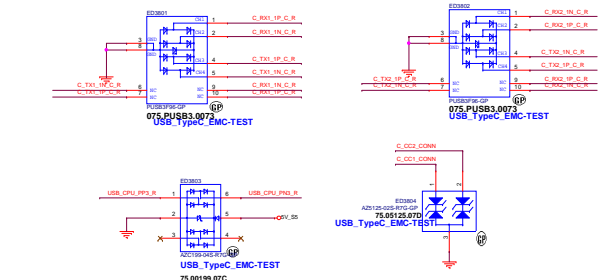
20170302  
check with vendor



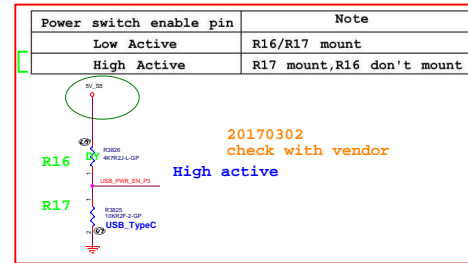
## USB Port3, Type C USB3.0 only



Close to CONN

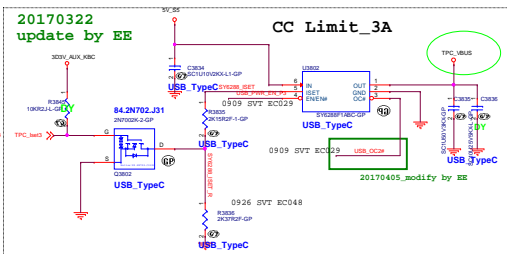
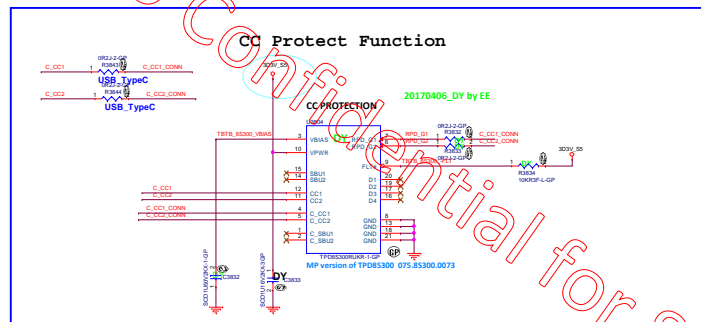
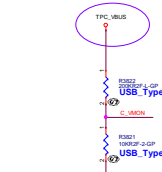


20170302  
check with vendor



20170302  
check with vendor

High active



1. AC: 15W/ 3A, 系統功耗不足降至4.5W/ 0.9A
2. DC: 4.5W/ 0.9A

### Over-current protection

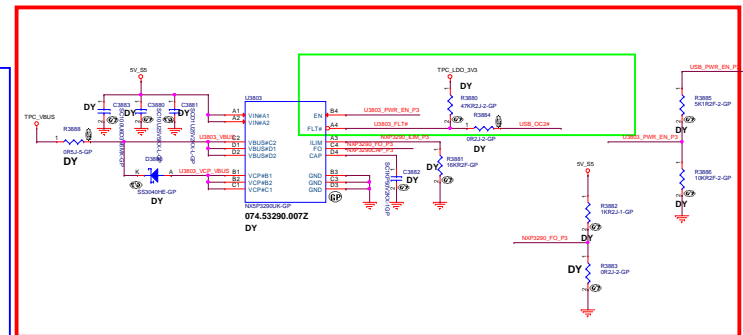
The SY6288F1/F2 supports Current limit programming. Connect a resistor  $R_{SET}$  from ISET pin to ground to program the current limit:

$$I_{LIM} (A) = 6800 / R_{SET} (\Omega)$$

The minimum current limit is 0.4A. Current limit beyond 4A is not recommended.

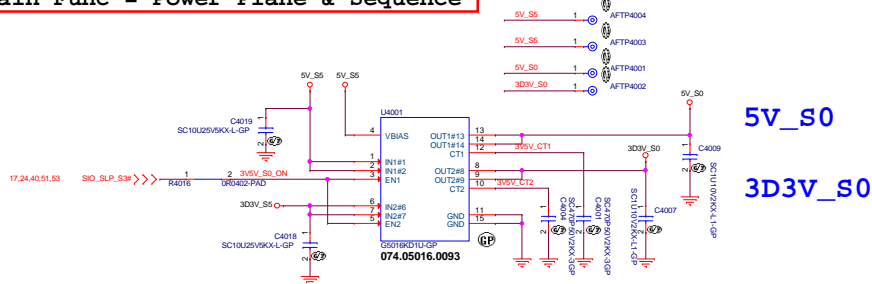
R3835/ 2.15K >> 3.16A  
R3835/ 2.15K + R3836/ 5.1K >> 0.94A

Power switch enable pin	Note
Low Active	R3826/R3825 mount
High Active	R3825 mount, R3826 don't mount



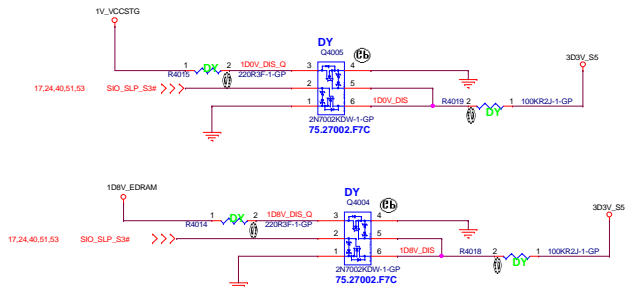
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<Variant Name>			
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Size	Document Number		Rev
A	Unicorn_LV530_KBL_MB14BOH01SA		1
Date:	Friday, December 15, 2017		Sheet 39 of 105

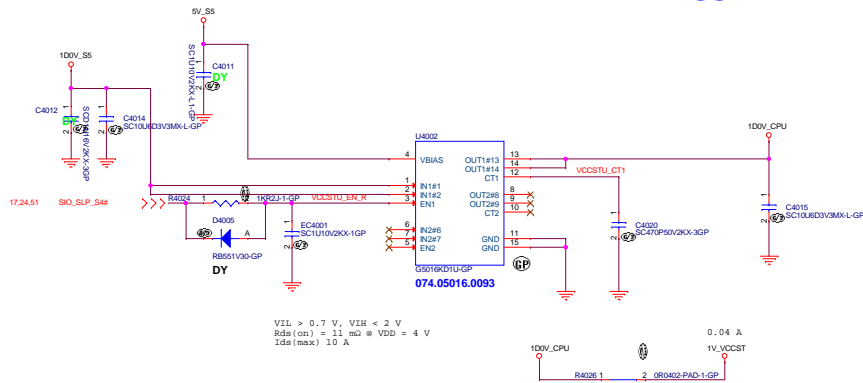


5V\_S0  
3D3V\_S0

### Discharge circuit



VCCST

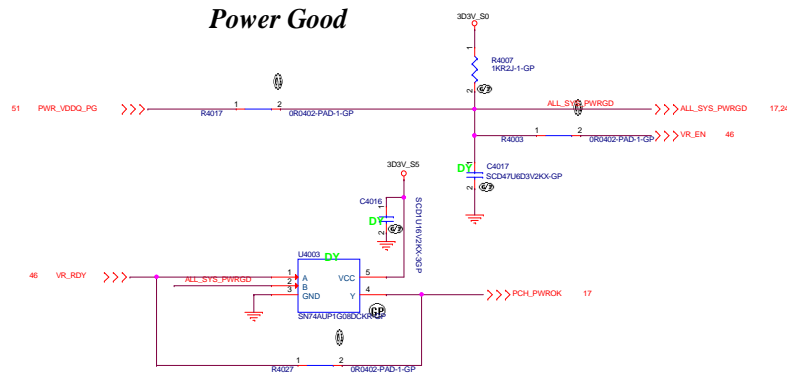


VIL > 0.7 V, VIH < 2 V  
Rds(on) = 11 mΩ @ VDS = 4 V  
Ids(max) 1.0 A

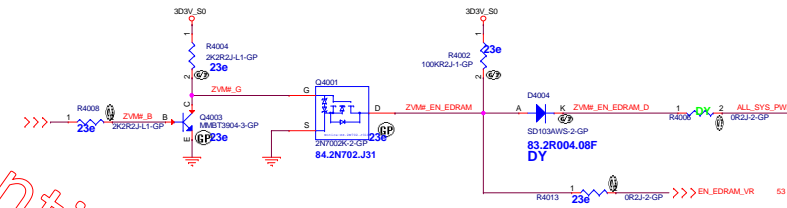
0.04 A

1V\_VCCST

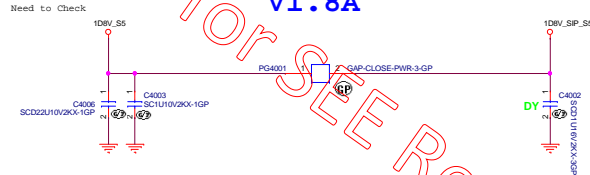
### Power Good



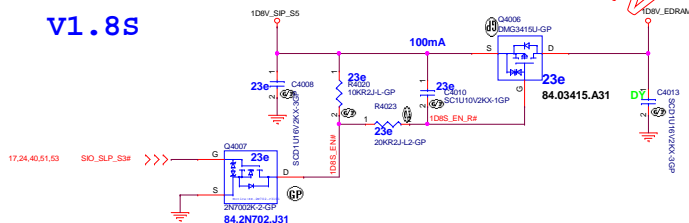
### GT3 Low Power Circuit (ZVM)



V1.8A



V1.8S



561280 KBL UY PDG Rev2.0 Notes:  
On power up sequence, VCCOPC\_ip8 must never ramp up after VCCOPC/VCCBOP10 under any circumstance.  
There are no ramp down requirements for VCCOPC\_ip8 and VCCOPC/VCCBOP10.  
Platform must guarantee VCCOPC/VCCBOP10 rails do not start ramping back up for any reason while VCCOPC\_ip8 is ramping down or OFF.

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<Variant Name>

Title <Title>			
Size A	Document Number <Doc>		Rev <RevCode>
Date:	Friday, December 15, 2017	Sheet 41 of 105	

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<Variant Name>

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Title			
<b>RESERVED</b>			
Size A4	Document Number		Rev
<b>Unicorn LV530 KBL MB</b>		<b>GA</b>	
Date: Friday, December 15, 2017		Sheet 42 of	105



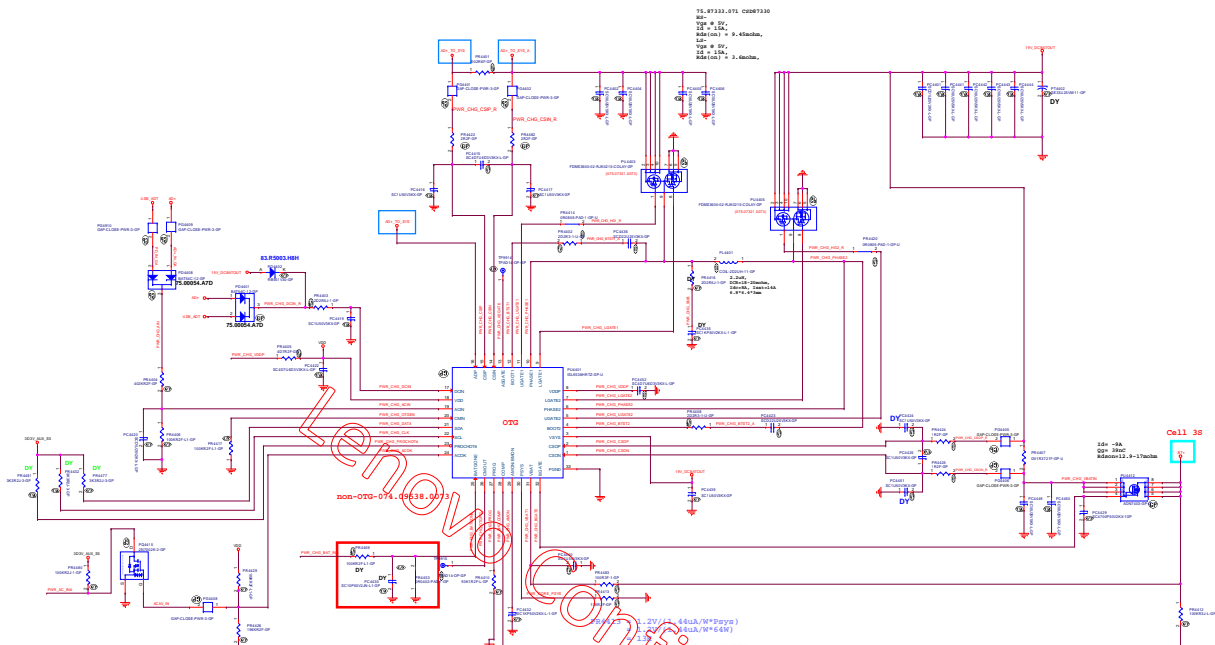
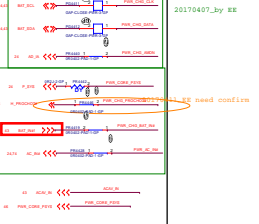


TABLE 65: PROG PIN PROGRAMMING OPTIONS

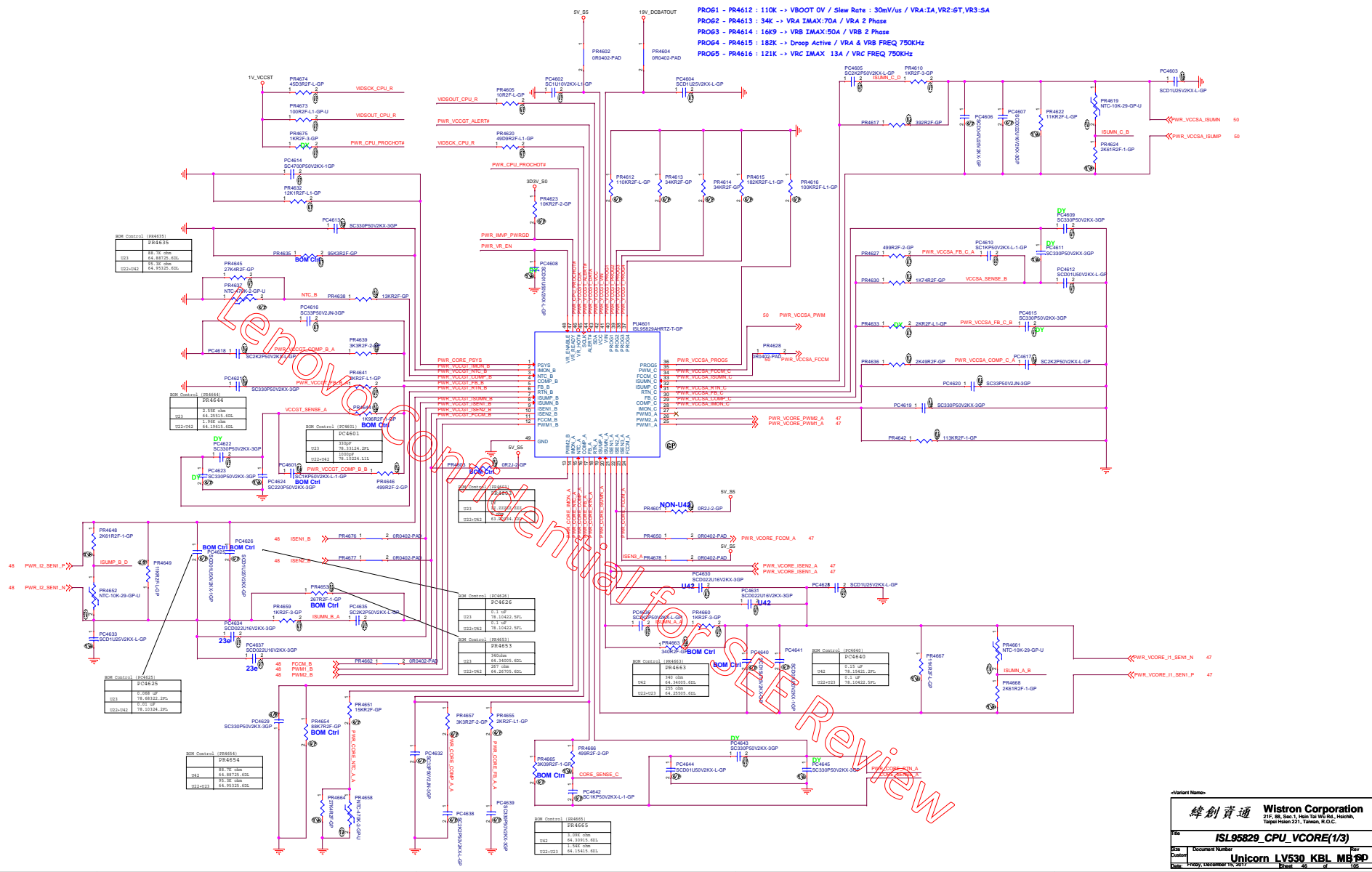
PROG PIN	RESISTANCE	MIN	MAX	DEFAULT
0	1	0	1	0.475
1	1	0	1	0.475
2	1	0	1	0.475
3	1	0	1	0.475
4	1	0	1	0.475
5	1	0	1	0.475
6	1	0	1	0.475
7	1	0	1	0.475
8	1	0	1	0.475
9	1	0	1	0.475
10	1	0	1	0.475
11	1	0	1	0.475
12	1	0	1	0.475
13	1	0	1	0.475
14	1	0	1	0.475
15	1	0	1	0.475
16	1	0	1	0.475
17	1	0	1	0.475
18	1	0	1	0.475
19	1	0	1	0.475
20	1	0	1	0.475
21	1	0	1	0.475
22	1	0	1	0.475
23	1	0	1	0.475
24	1	0	1	0.475
25	1	0	1	0.475
26	1	0	1	0.475
27	1	0	1	0.475
28	1	0	1	0.475
29	1	0	1	0.475
30	1	0	1	0.475
31	1	0	1	0.475
32	1	0	1	0.475
33	1	0	1	0.475
34	1	0	1	0.475
35	1	0	1	0.475
36	1	0	1	0.475
37	1	0	1	0.475
38	1	0	1	0.475
39	1	0	1	0.475
40	1	0	1	0.475
41	1	0	1	0.475
42	1	0	1	0.475
43	1	0	1	0.475
44	1	0	1	0.475
45	1	0	1	0.475
46	1	0	1	0.475
47	1	0	1	0.475
48	1	0	1	0.475
49	1	0	1	0.475
50	1	0	1	0.475
51	1	0	1	0.475
52	1	0	1	0.475
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55	1	0	1	0.475
56	1	0	1	0.475
57	1	0	1	0.475
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59	1	0	1	0.475
60	1	0	1	0.475
61	1	0	1	0.475
62	1	0	1	0.475
63	1	0	1	0.475
64	1	0	1	0.475
65	1	0	1	0.475
66	1	0	1	0.475
67	1	0	1	0.475
68	1	0	1	0.475
69	1	0	1	0.475
70	1	0	1	0.475
71	1	0	1	0.475
72	1	0	1	0.475
73	1	0	1	0.475
74	1	0	1	0.475
75	1	0	1	0.475
76	1	0	1	0.475
77	1	0	1	0.475
78	1	0	1	0.475
79	1	0	1	0.475
80	1	0	1	0.475
81	1	0	1	0.475
82	1	0	1	0.475
83	1	0	1	0.475
84	1	0	1	0.475
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86	1	0	1	0.475
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88	1	0	1	0.475
89	1	0	1	0.475
90	1	0	1	0.475
91	1	0	1	0.475
92	1	0	1	0.475
93	1	0	1	0.475
94	1	0	1	0.475
95	1	0	1	0.475
96	1	0	1	0.475
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100	1	0	1	0.475

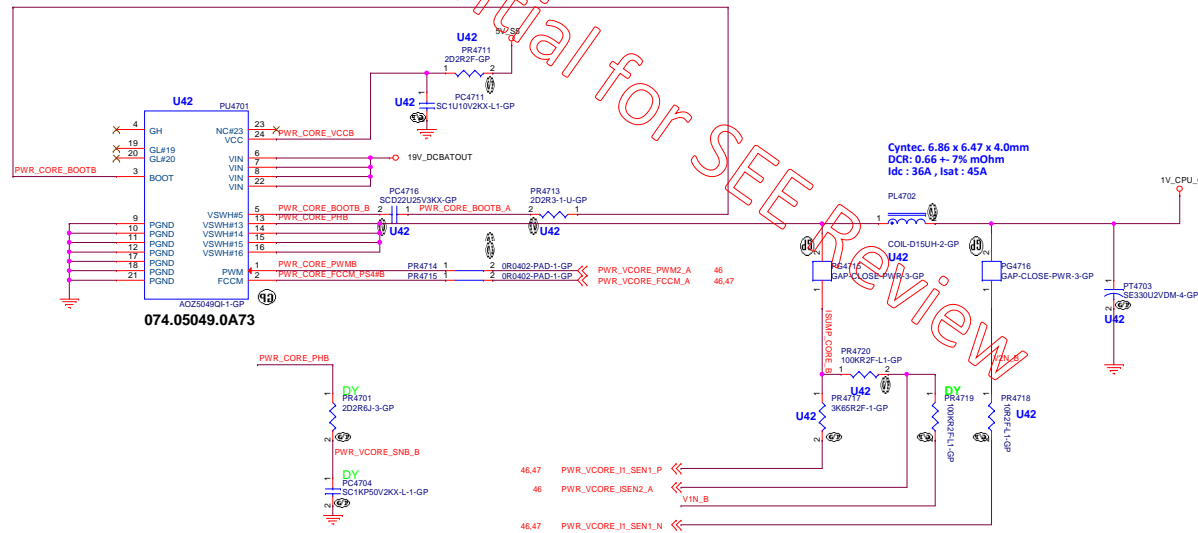
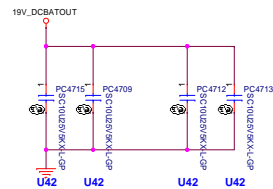
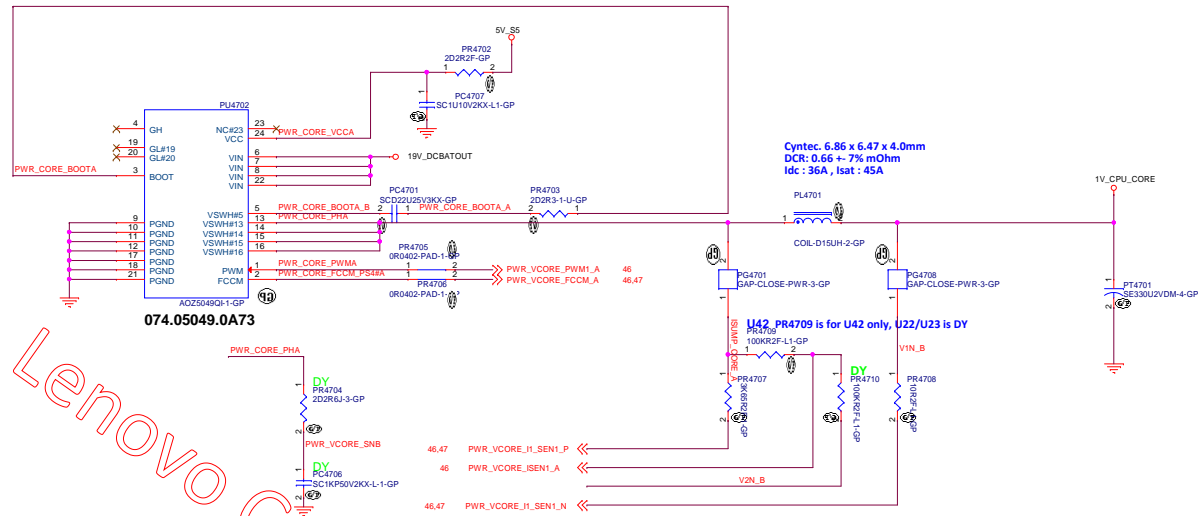
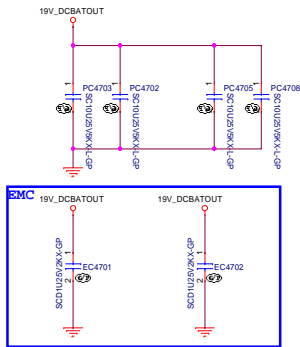


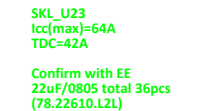
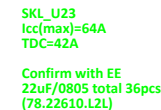
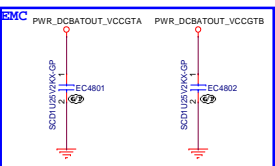


OFFPAGE

H_PROCHOT#	PR4652 1 DR0402-PAD	3	PWR_CPU_PROCHOT#
EVD_ALERT#_CPU	PR4608 1 DR0402-PAD	2	PWR_VCCOUT_ALERT#
SVID_CLK_CPU	PR4621 1 DR0402-PAD	2	VDSBCK_CPU_R
SVID_DATA_CPU	PR4618 1 DR0402-PAD	2	VDSOUT_CPU_R
VR_IDY	PR4660 1 DR0402-PAD	2	PWR_MVP_PWMRD
VR_EN	PR4663 1 DR0402-PAD	2	PWR_VR_EN
VBS_SENSE	PR4620 1 DR0402-PAD	2	PWR_CORE_RTN_A
VCC_SENSE	PR4671 1 DR0402-PAD	2	CORE_SENSE_A
VCCOUT_SENSE	PR4606 1 DR0402-PAD	2	VCCOUT_SENSE_A
VDSOUT_SENSE	PR4602 1 DR0402-PAD	2	PWR_VCCOUT_RTN_B
VSSA_SENSE	PR4629 1 DR0402-PAD	2	PWR_VCCSA_RTN_C
VCCSA_SENSE	PR4631 1 DR0402-PAD	2	VCCSA_SENSE_B
PWR_CORE_PSYS	PR4605 1 DR0402-PAD	2	PWR_CORE_PSYS



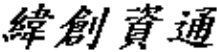




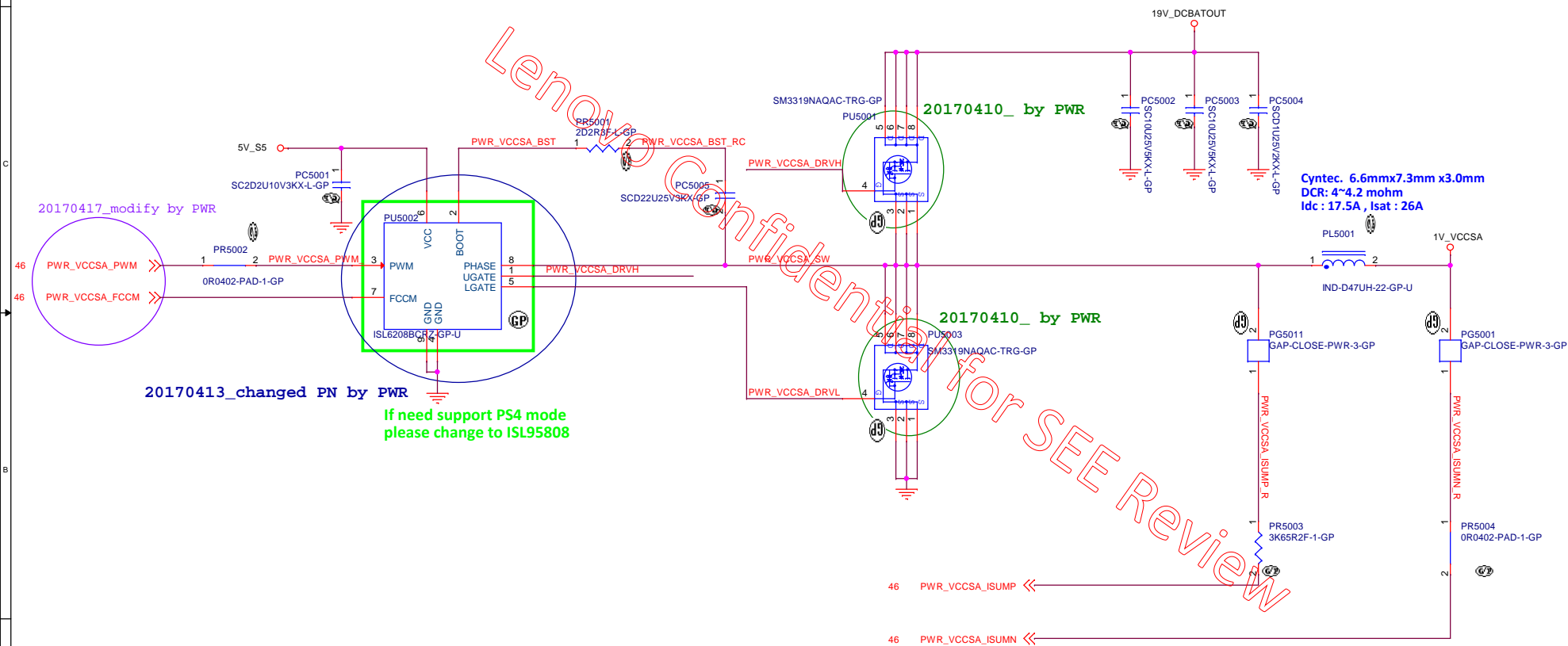
Lenovo Confidential for SEE Review

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Title <b>CPU_VCCGTUS</b>			
Size A4	Document Number <b>Unicorn LV530 KBL MB 6A</b>		Rev <b>1A</b>
Date: Friday, December 15, 2017		Sheet 49 of	105

Main Func = CPU\_CORE



<Variant Name>

緯創資通

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU\_VCCGTUS

Size  
A3

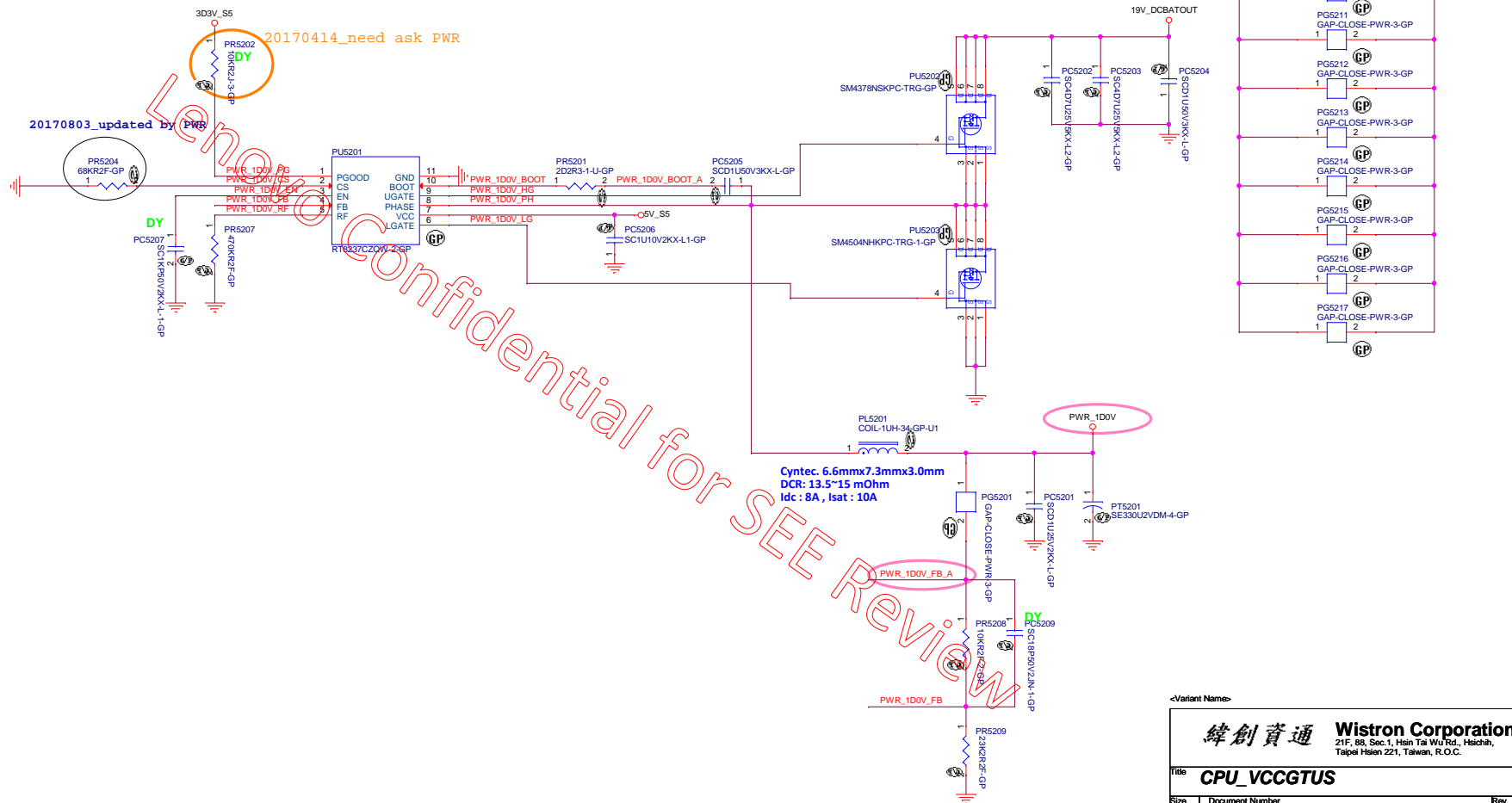
Document Number

Unicorn LV530 KBL MB14A

Date: Friday, December 15, 2017

Sheet 50 of 105

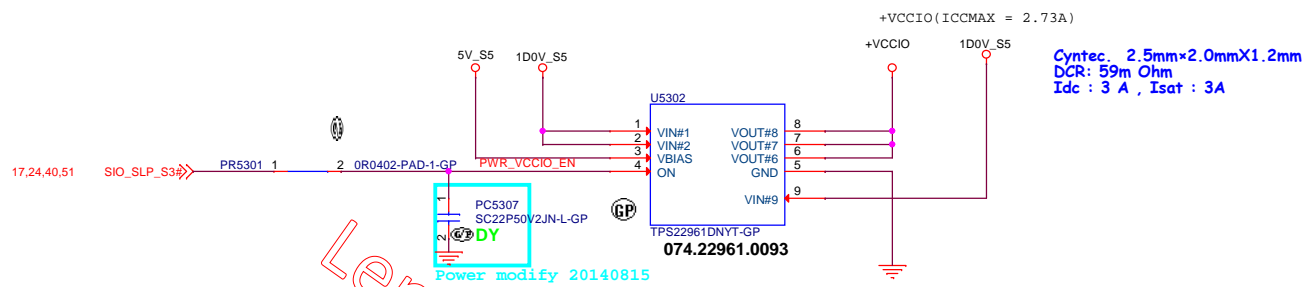




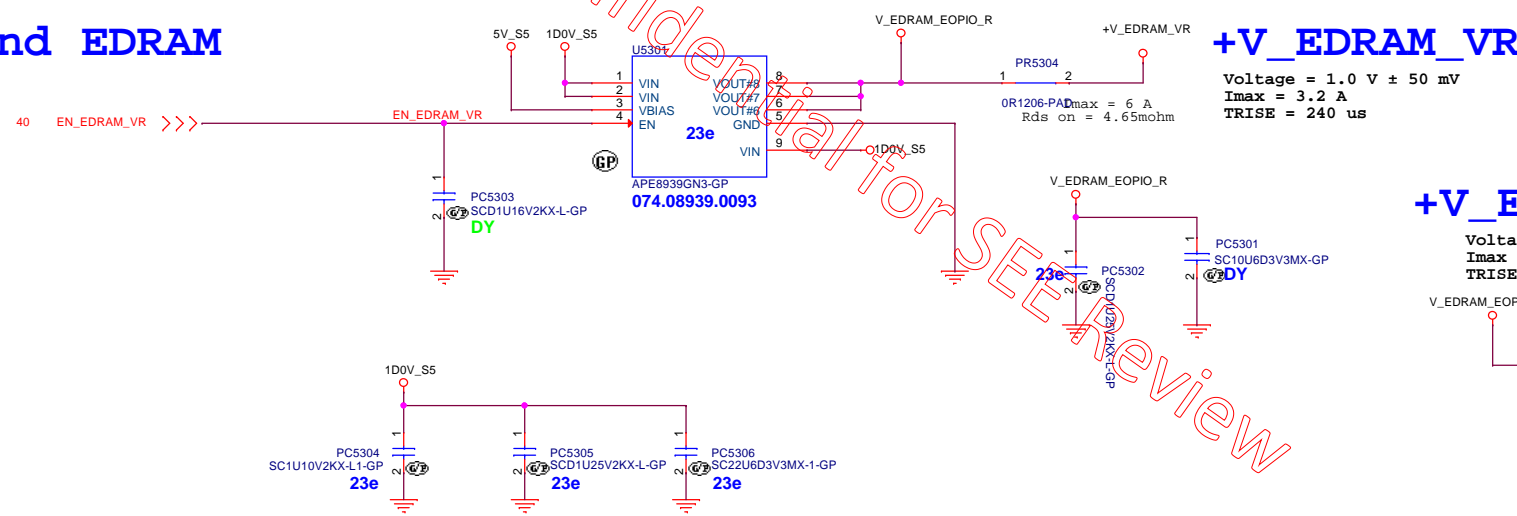


Main Func = 1D0V

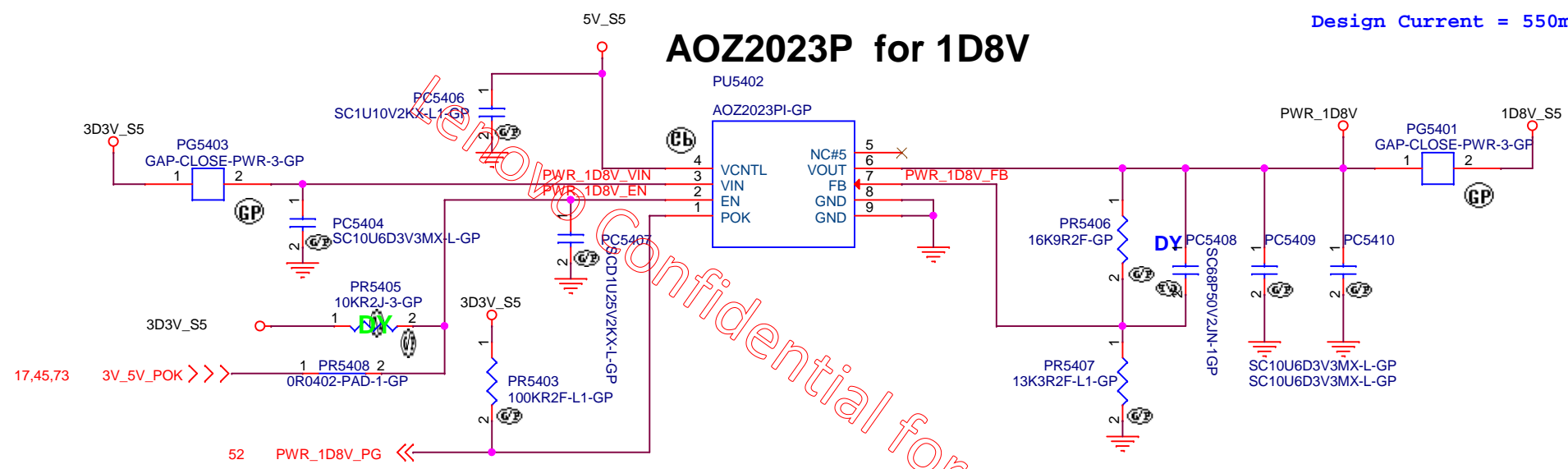
VCCIO



EOPIO and EDRAM



Main Func = 1D8V



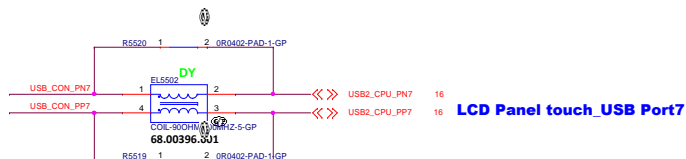
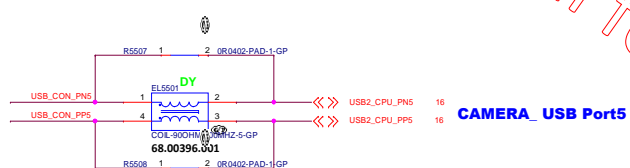
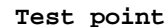
$$V_{out} = 0.8V * (R1 + R2) / R2$$
  
<Variant Name>

<b>緯創資通</b>			<b>Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
<b>RT9025 1D8V</b>					
Size	Document Number				Rev
A4	<b>Unicorn LV530 KBL MB</b>				<b>64</b>
Date:	Friday, December 15, 2017		Sheet	54	of 105

20170427  
need check pin define

need check pin define

### INVERTER POWER

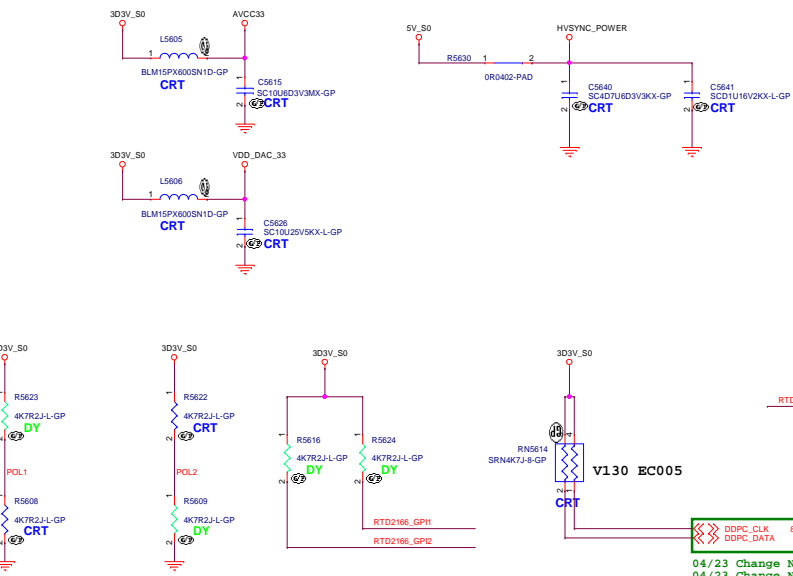
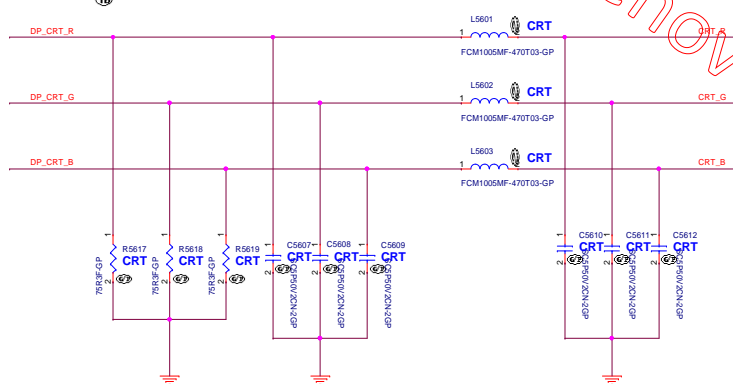


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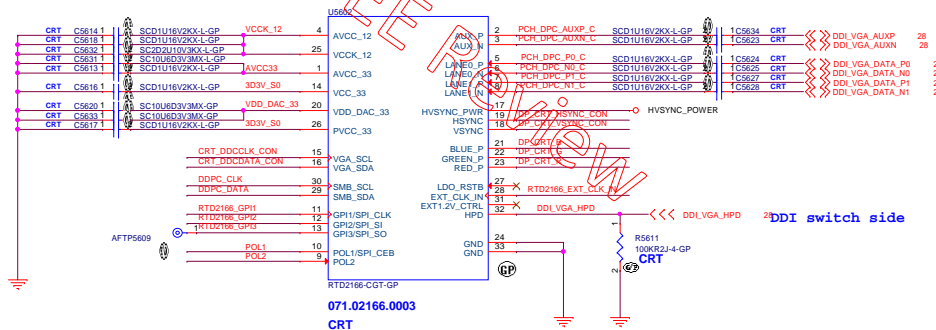
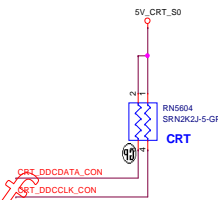
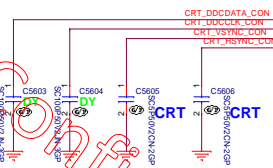
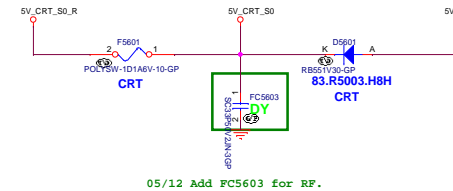
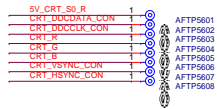
Shark Bay SV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ODD(Reserved)			
Size	Document Number		Rev
A3	Unicorn LV530 KBL MB13A		1A
Date: Friday, December 15, 2017		Sheet 56 of	105





LAYOUT NOTE:  
All cap need close to chip  
especially C616 close pin5  
C618 and C619 close pin19  
C620 and C621 close pin9  
C617 close pin20  
C614 close pin25  
C613 lose pin24



DDI switch side

```
04/23 Change Net Name to DDP_C_CLK
04/23 Change Net Name to DDP_C_DATA
```

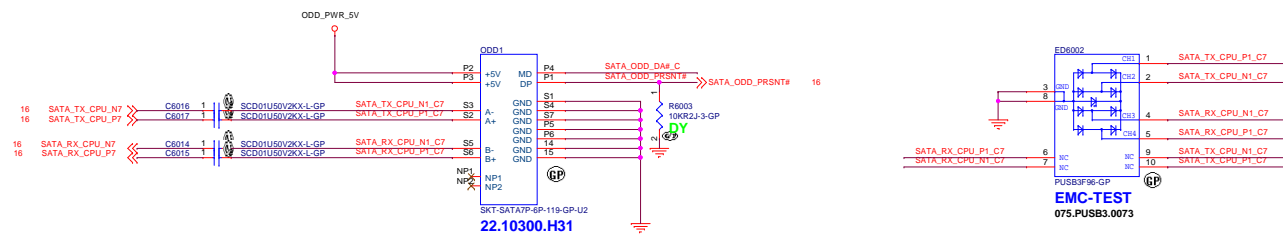
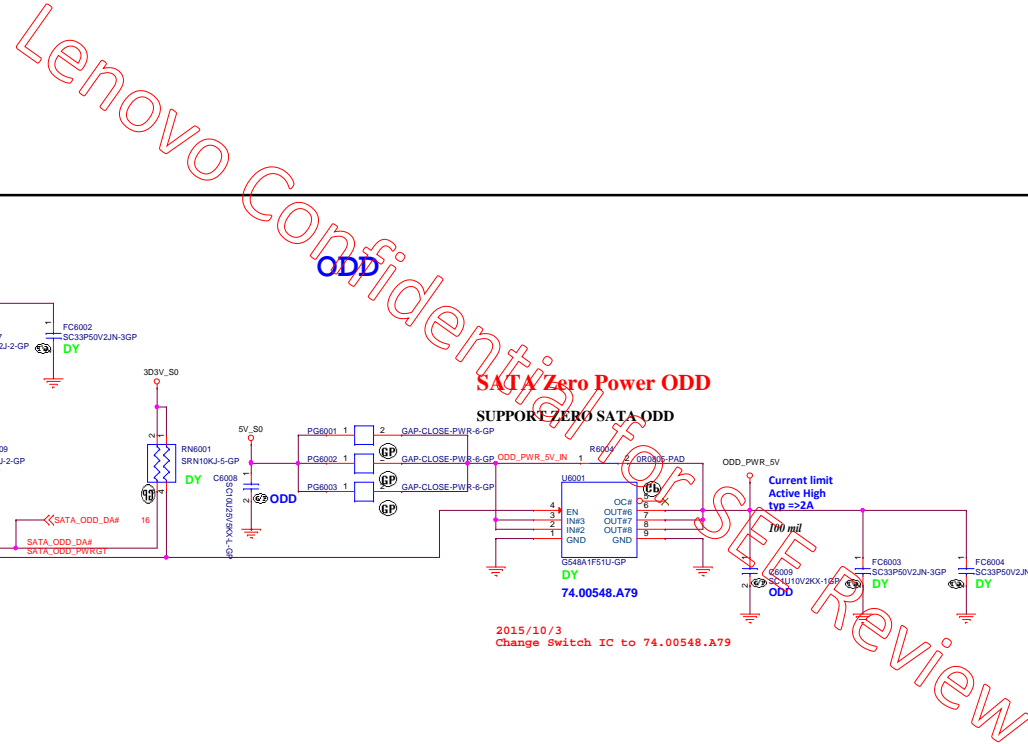
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BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>RESERVED</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>Unicorn LV530 KBL MB</div>		<div>1A</div>
<div>Date: Friday, December 15, 2017</div>		<div>Sheet</div>	<div>59 of 105</div>

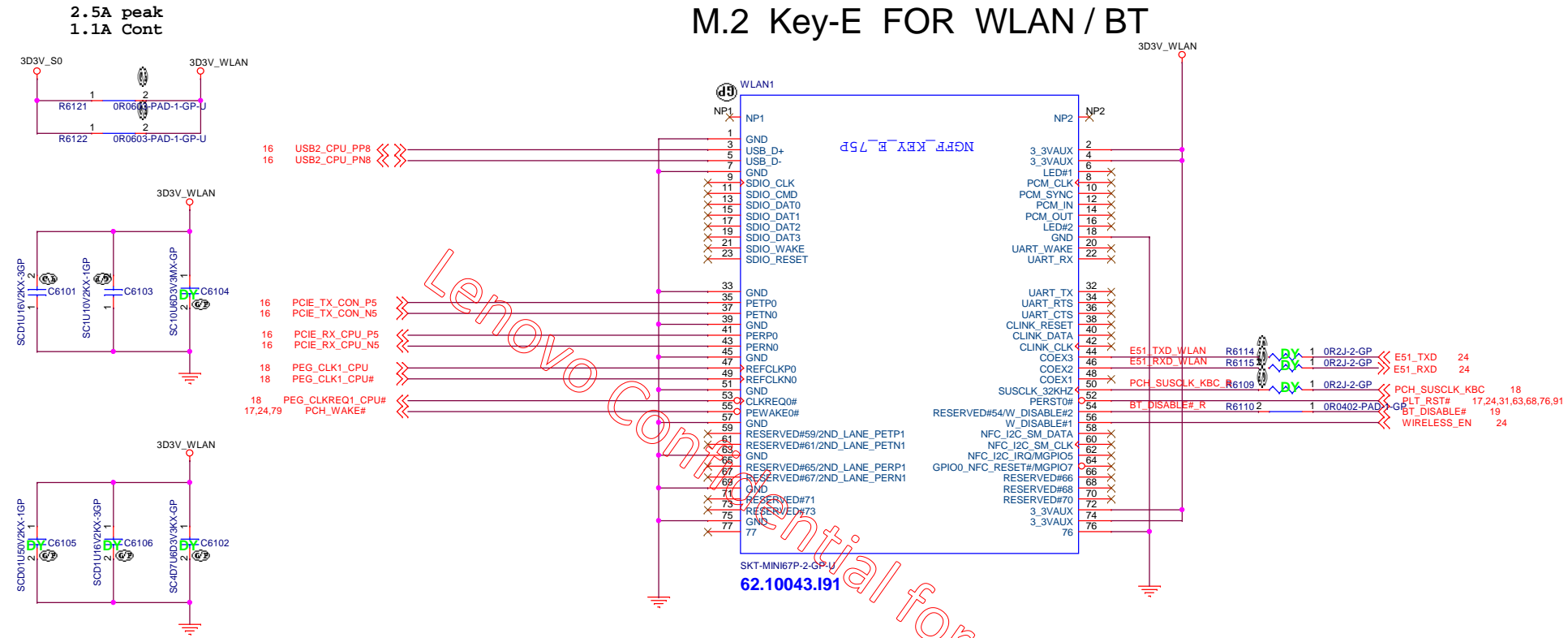
**HDD** 20170427  
Cnchange pin define follow LV315ST(NC) but pn 1 different





Main Func = WLAN

M.2 Key-E FOR WLAN / BT

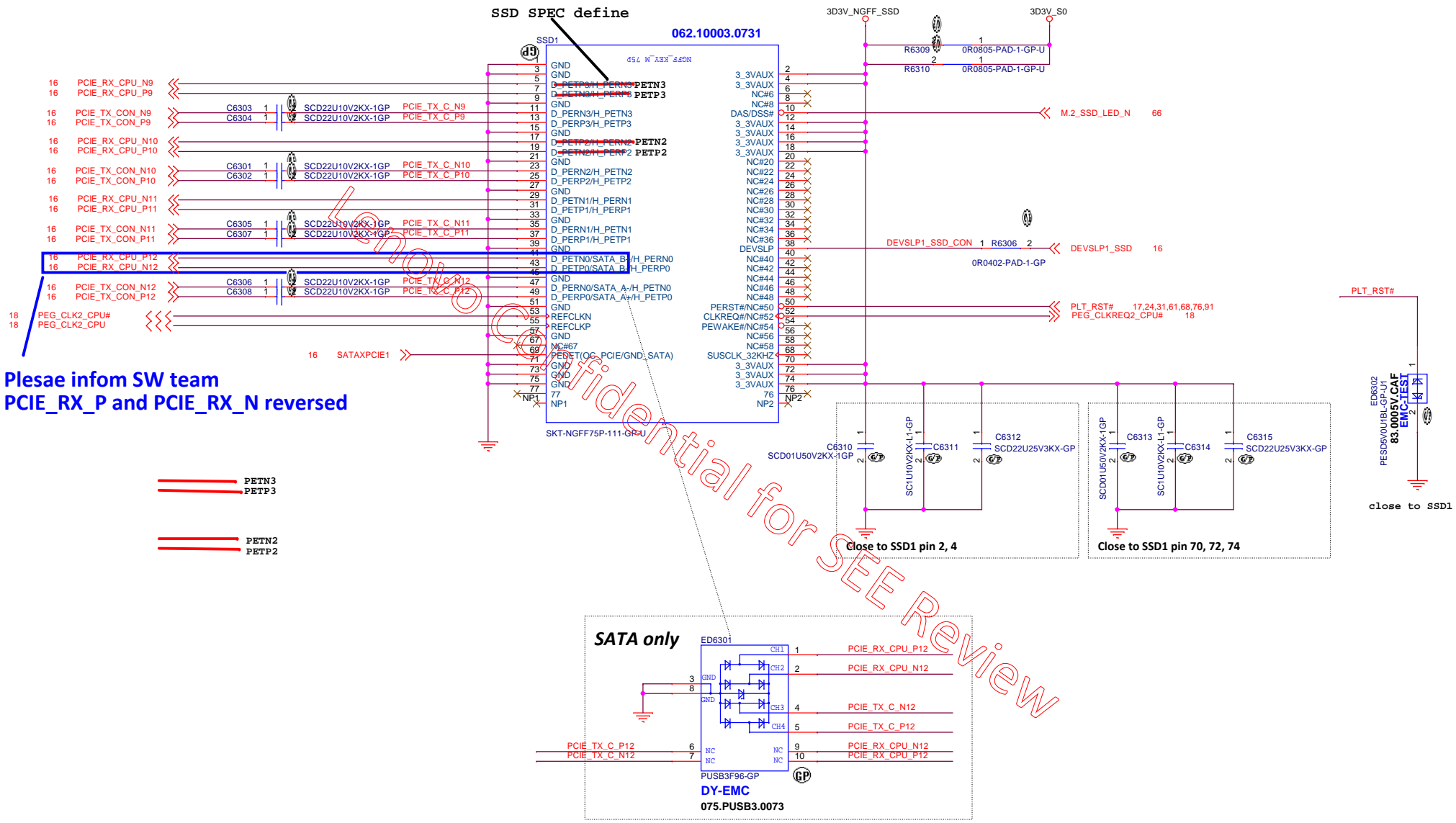


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Confidential for SEE Review

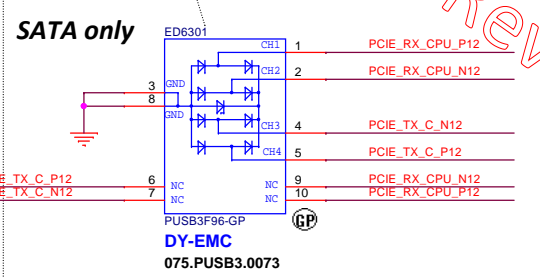
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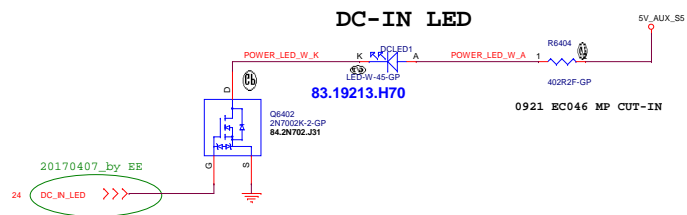
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
Size	Document Number		Rev
A4	Unicorn LV530 KBL MB		64
Date: Friday, December 15, 2017		Sheet 62 of	105

Main Func = SSD TYPE-M NGFF CARD FOR PCIE SSD/Optane

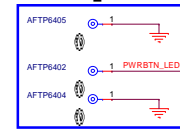


Plesae infom SW team  
PCIE\_RX\_P and PCIE\_RX\_N reversed

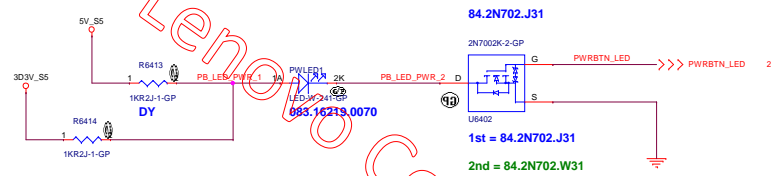




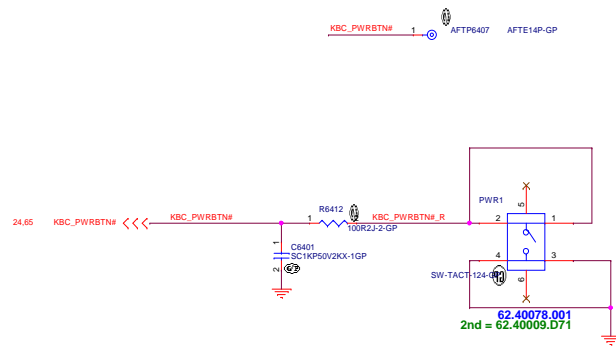
### Test point



### POWER BTN LED



### KBC\_PWRBTN#



BOM1

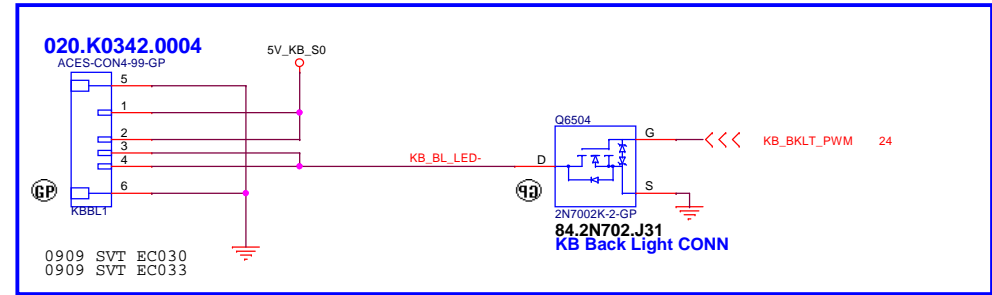
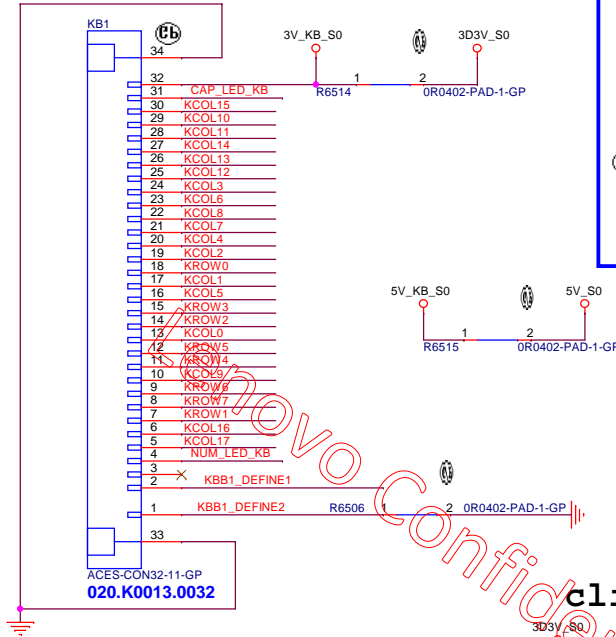
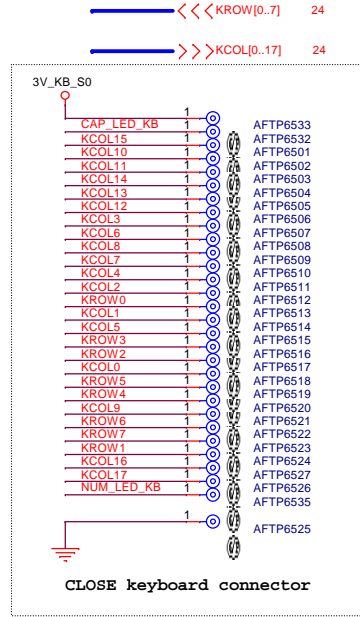
**緯創資通 Wistron Corporation**  
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichuan,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LED / POWER BUTTON			
Size	Document Number	Rev	
A2	Unicorn LV530 KBL_MB14	SA	
Date: Friday, December 15, 2017 Sheet 64 of 106			

# SSID = Touch.Pad

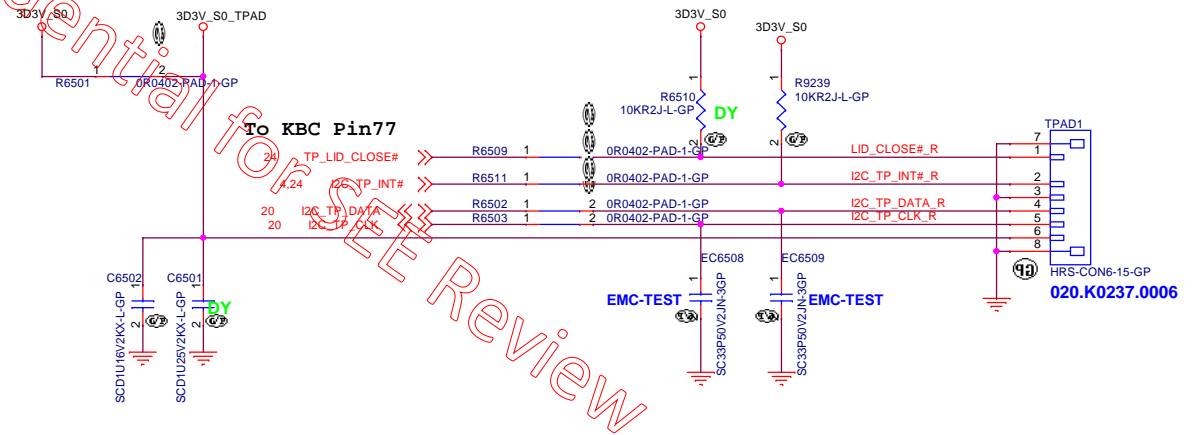
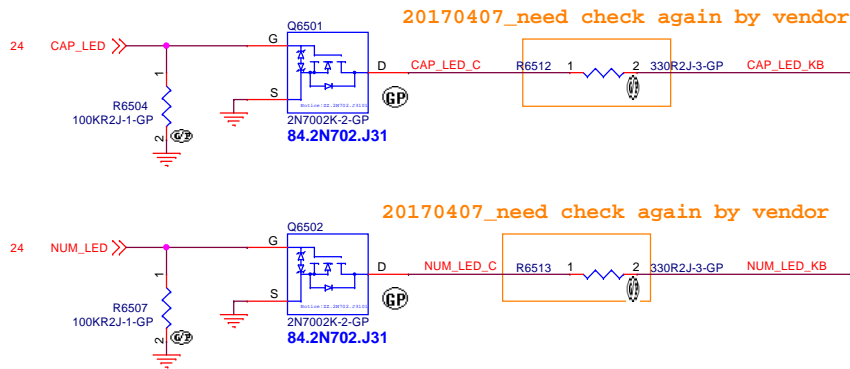
20170427\_pin deifne check by Dennis

## KB\_LED

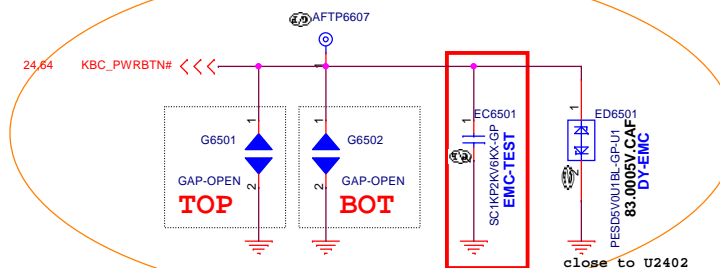


## click pad

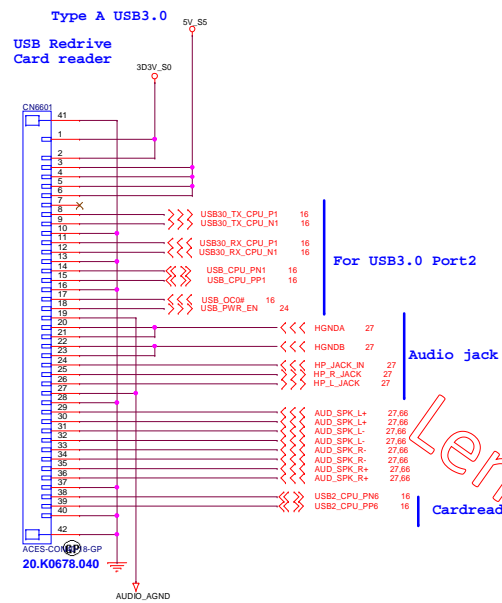
20170421  
Cnhange pin define by Dennis



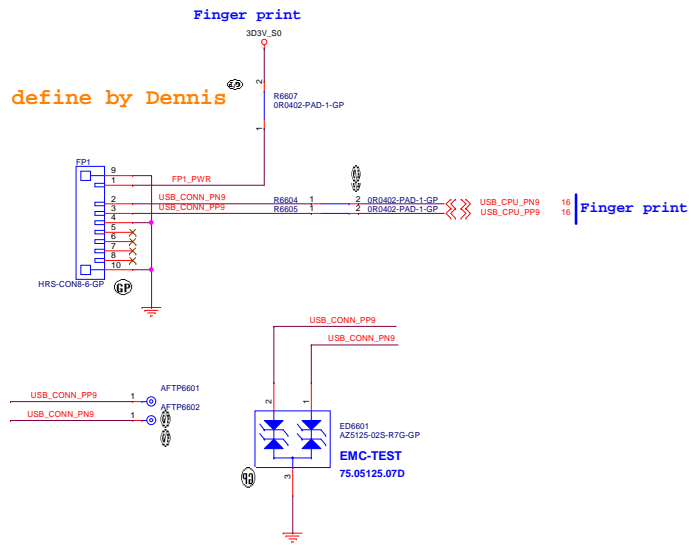
20170412\_ WKS test by LB720



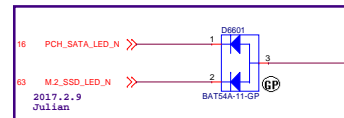
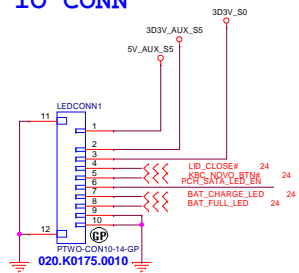
## 10 CONN



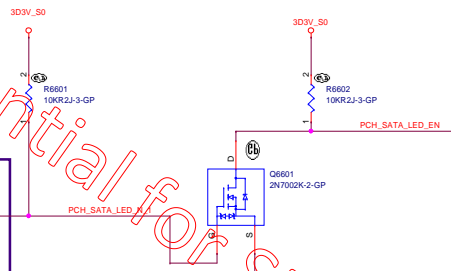
20170421  
Cnchange pin define by Dennis



LED IO CONN



LOW:ENABLE, LED ON  
HIGH:DISABLE,LED OFF



BOM1			
<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 8F, Sec. 1, Hsin Tsu Wu Rd., Hsichih, Taipei Hsien 221, Taiwan R.O.C.	
<b>LEDIO IO BOARD CONN</b>			
Title			
Size	Document Number		Rev
A2	<b>Unicorn LV530_KBL_MB14</b>		1/1
Date	Friday, December 15, 2017	Sheet	6B of 10

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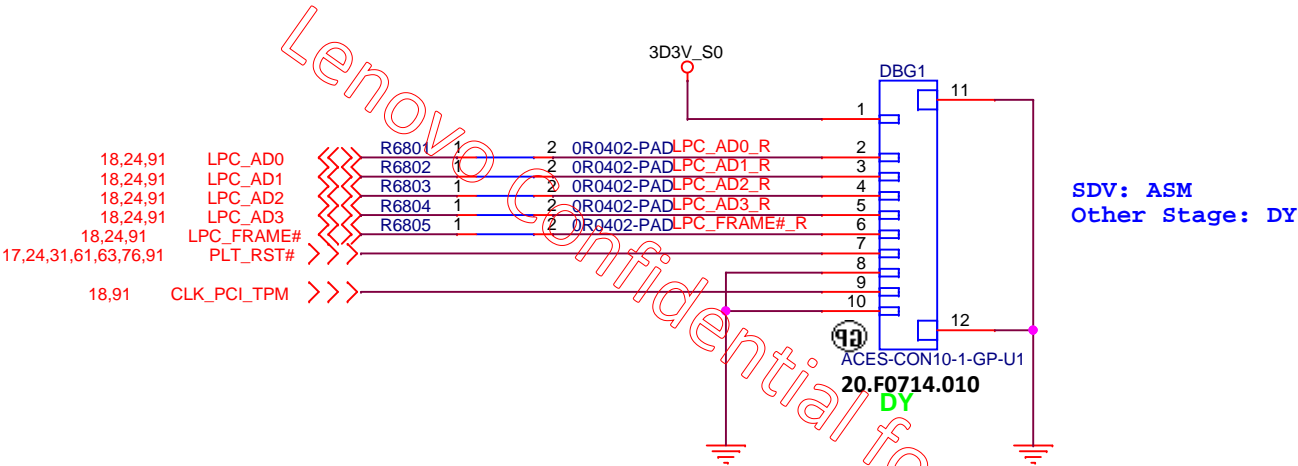
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BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>RESERVED</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>Unicorn LV530 KBL MB</div>		<div>6A</div>
<div>Date: Friday, December 15, 2017</div>		<div>Sheet 67 of 105</div>	

Main Func = Debug

Debug Connector



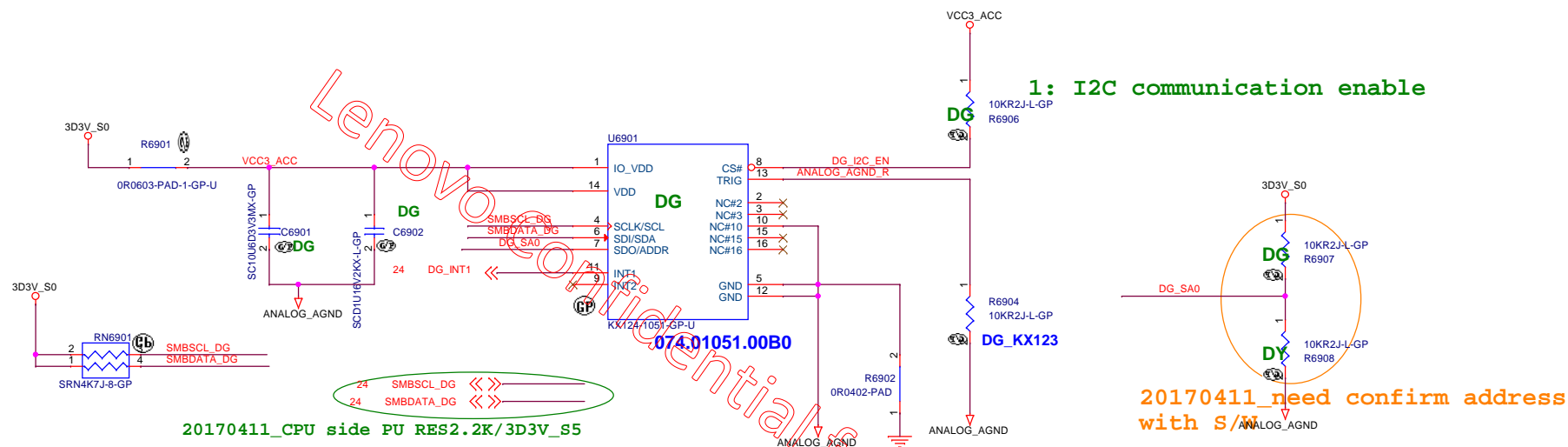
BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
DEBUG CONN			
Size	Document Number	Rev	
A4	Unicorn_LV530_KBL_MB14	SA	
Date:	Friday, December 15, 2017	Sheet	68 of 105



# G-Sensor

1st:ST/ LIS3DETR, 74.00003.BB0  
(cannot be used, bit not enough)  
2nd:KX124-1051, 074.01051.00B0



M40

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
G Sensor			
Size	Document Number		Rev
A3	Unicorn LV530 KBL_MB14		SA
Date:	Friday, December 15, 2017	Sheet 69 of	105

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BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
Size	Document Number		Rev
A4	Unicorn LV530 KBL MB 6A		1A
Date: Friday, December 15, 2017		Sheet 70 of 105	

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BOM1

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Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size  
A4

Document Number

Rev

Unicorn LV530 KBL MB 1A

Date: Friday, December 15, 2017

Sheet 71 of 105

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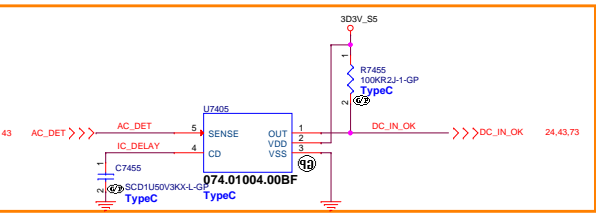
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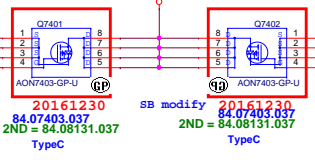
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date: Friday, December 15, 2017		Sheet 72 of 105

VCCPD\_VBUS\_CONN LDO\_3V3 3D3V\_S5

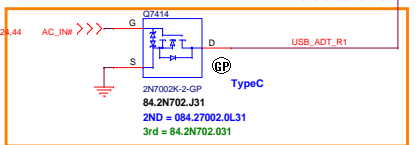




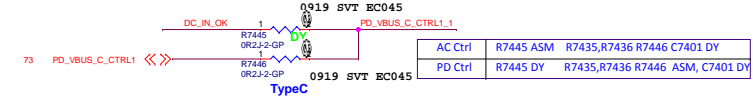
USB PD (Consumer: 20V 3.25A, Provider: 5V 2A)  
To System



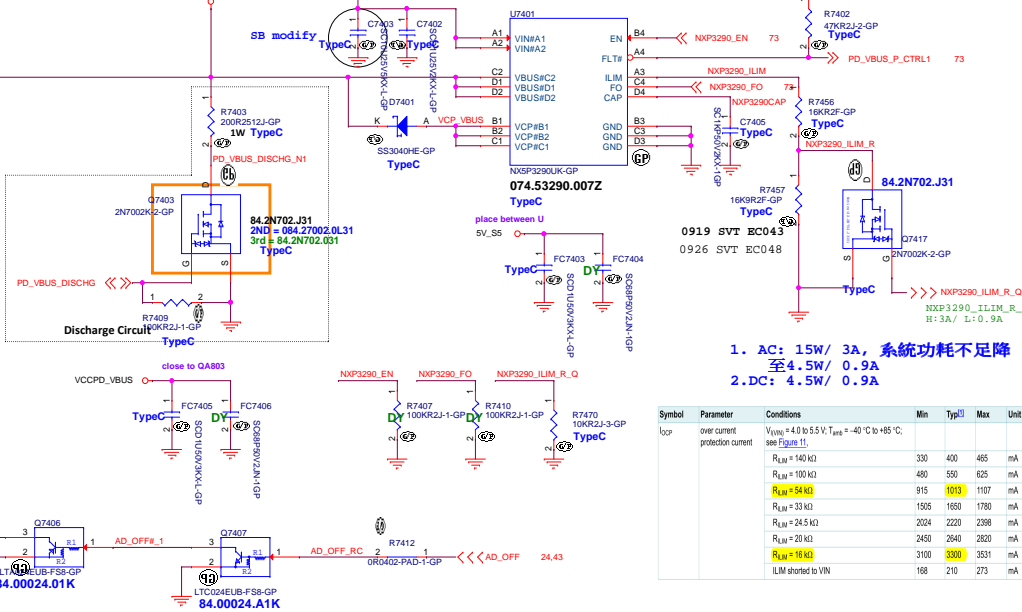
VBUS\_C\_CTRL = 0 (Consumer Path ON)  
VBUS\_C\_CTRL = 1 (Consumer Path OFF)



Battery charger will turn off QA802 without any adapter in

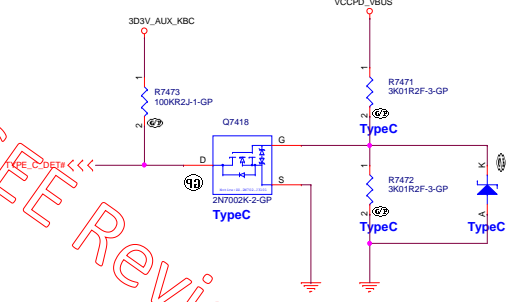


19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4302	ON	Control by DC_IN_OK or ACAV_IN
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	Control by BGATE
					PU4302	OFF	
					PU4412	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					PU4302	ON	
					PU4412	OFF	
Battery Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4302	OFF	
					PU4412	ON	Battery to 19V_DCBATOUT



1. AC: 15W/ 3A, 系統功耗不足降  
至 4.5W/ 0.9A  
2. DC: 4.5W/ 0.9A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Iscr	over current protection current	V <sub>IN</sub> = 4.0 to 5.5V, T <sub>amb</sub> = -40 °C to +85 °C, see Figure 15				
		R <sub>DS(on)</sub> = 140 mΩ	330	400	465	mA
		R <sub>DS(on)</sub> = 100 mΩ	440	550	625	mA
		R <sub>DS(on)</sub> = 33 mΩ	915	1035	1107	mA
		R <sub>DS(on)</sub> = 24.5 mΩ	1595	1650	1760	mA
		R <sub>DS(on)</sub> = 20 mΩ	2024	2220	2368	mA
		LIM shorted to VIN	2450	2640	2820	mA
			3100	3300	3531	mA



BOM1

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title TYPEC PD Controller

Size Document Number

Custom Unicorn LV530\_KBL\_MB14

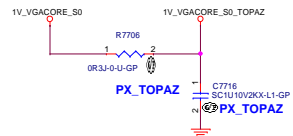
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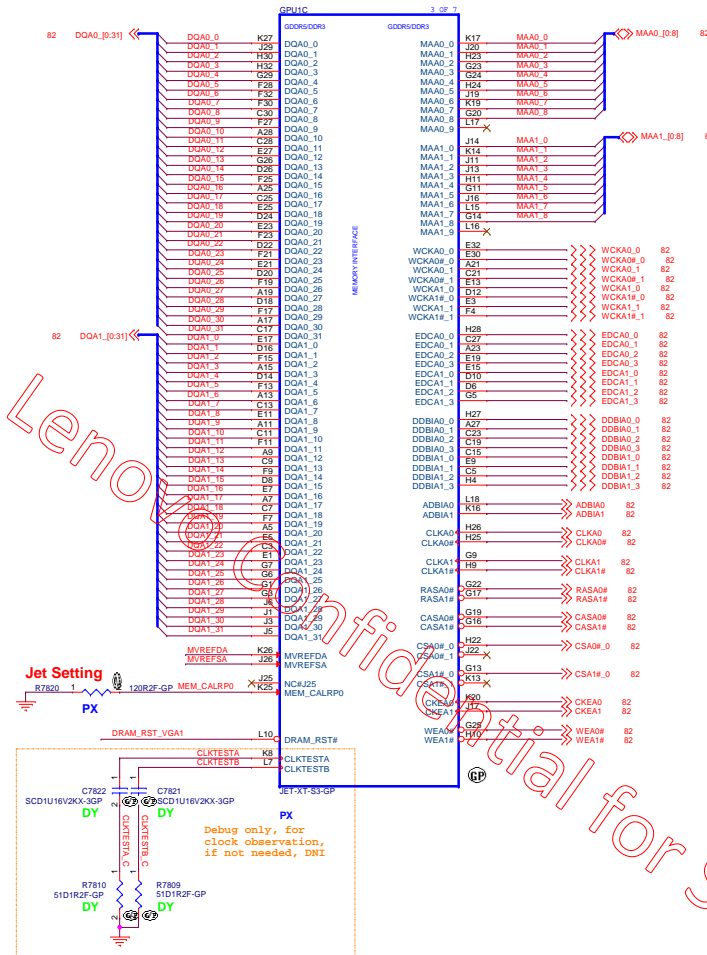
Rev SA

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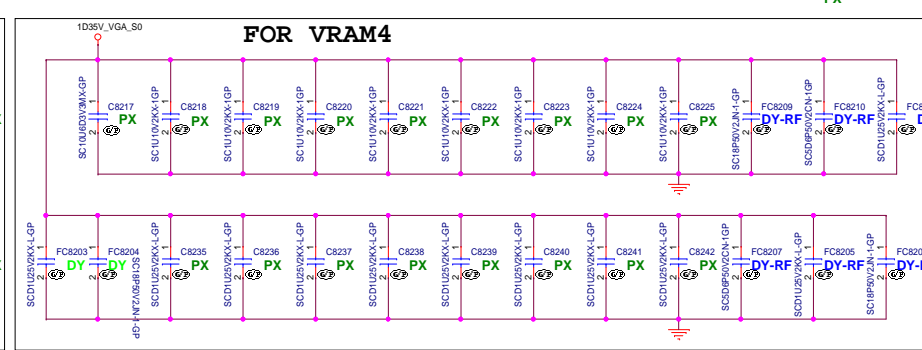
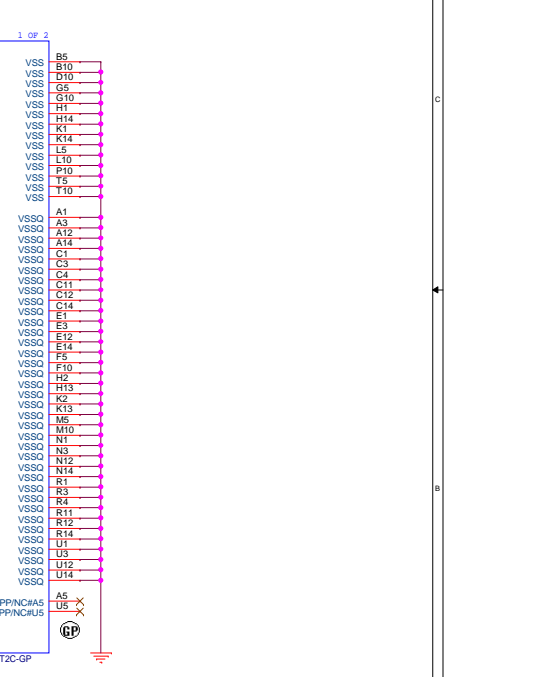
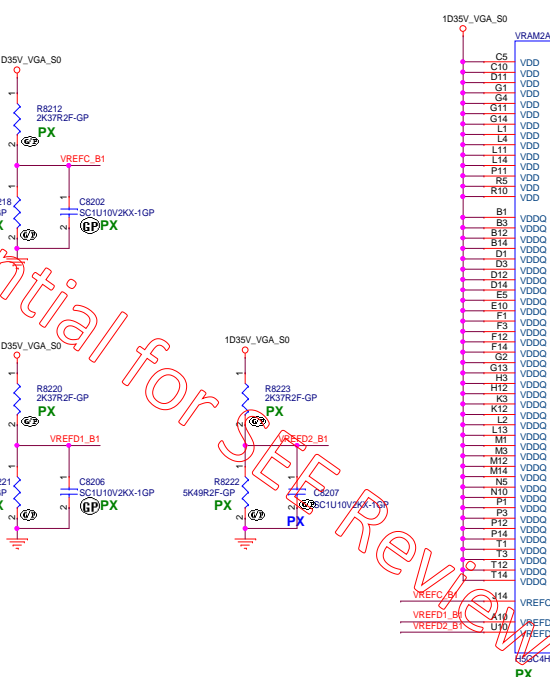
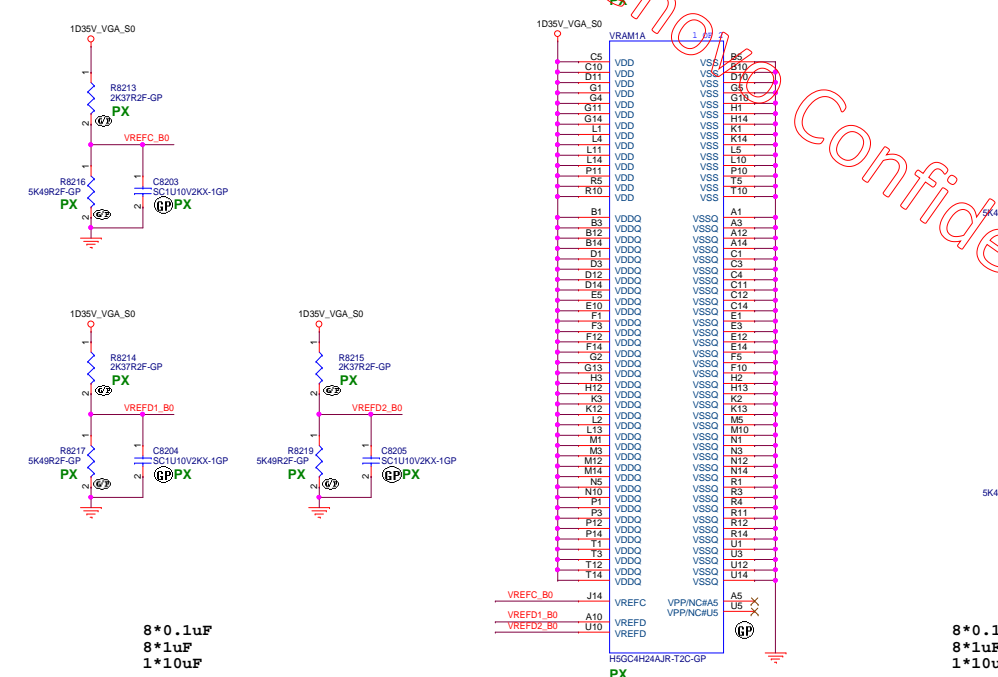






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BOM1		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleGPU VRAM1,2 (1/4)		
SizeC	Document NumberUnicorn LV530 KBL MB14	RevSA
Date: Friday, December 15, 2017Sheet 81 of 105		



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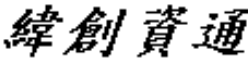
BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
Size	Document Number		Rev
A	Unicorn LV530 KBL MB15A		1A
Date:	Friday, December 15, 2017		Sheet 83 of 105

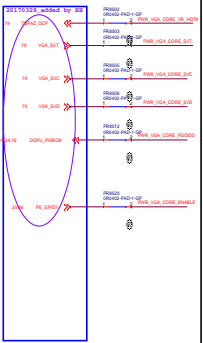
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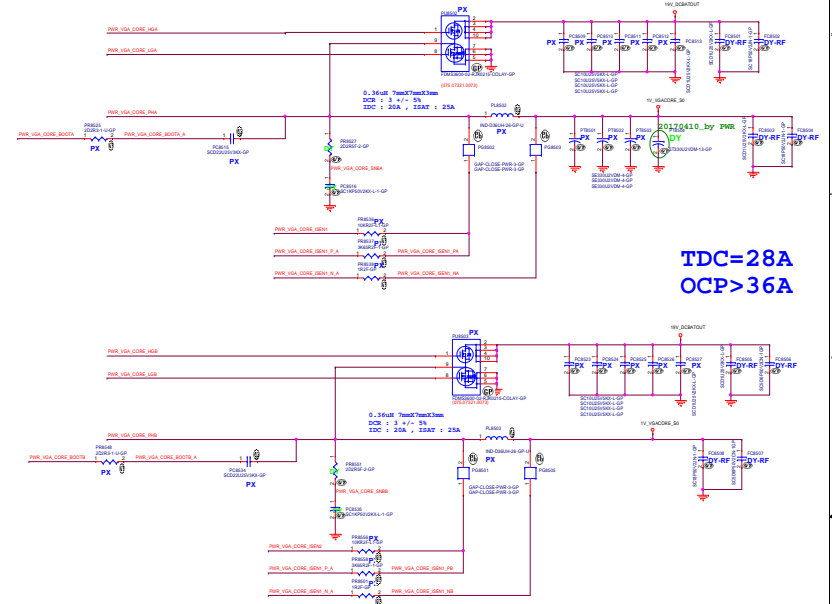
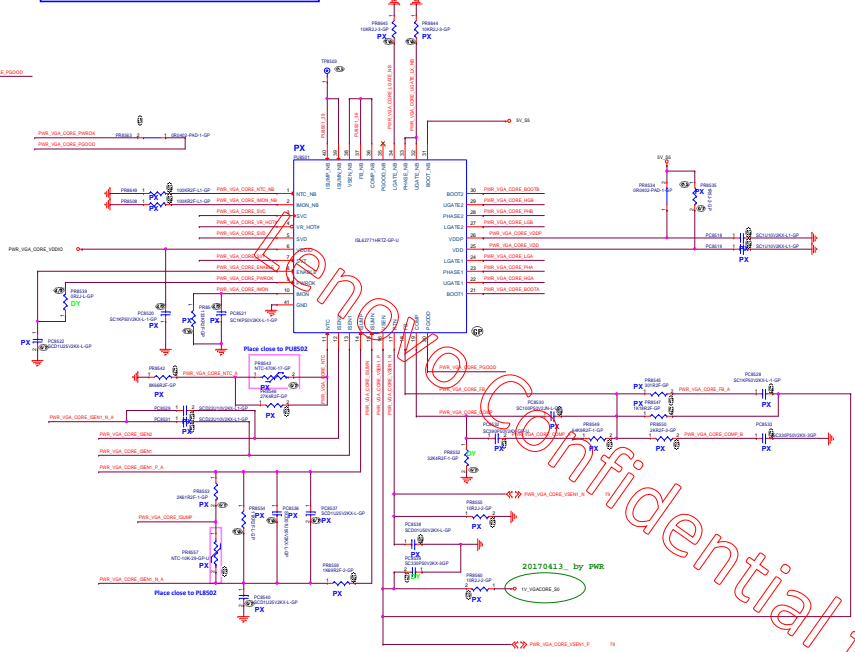
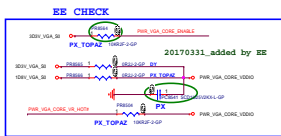
BOM1

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU VRAM7,8 (4/4)</b>			
Size	Document Number		Rev
A	<b>Unicorn LV530 KBL MB19A</b>		1A
Date:	Friday, December 15, 2017		Sheet 84 of 105





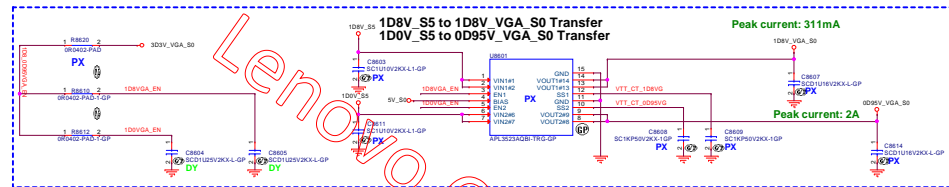
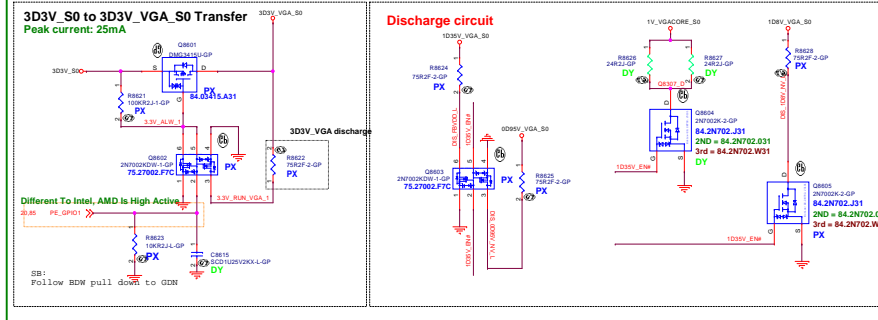
EE CHECK



TDC=28A  
OCP>36A

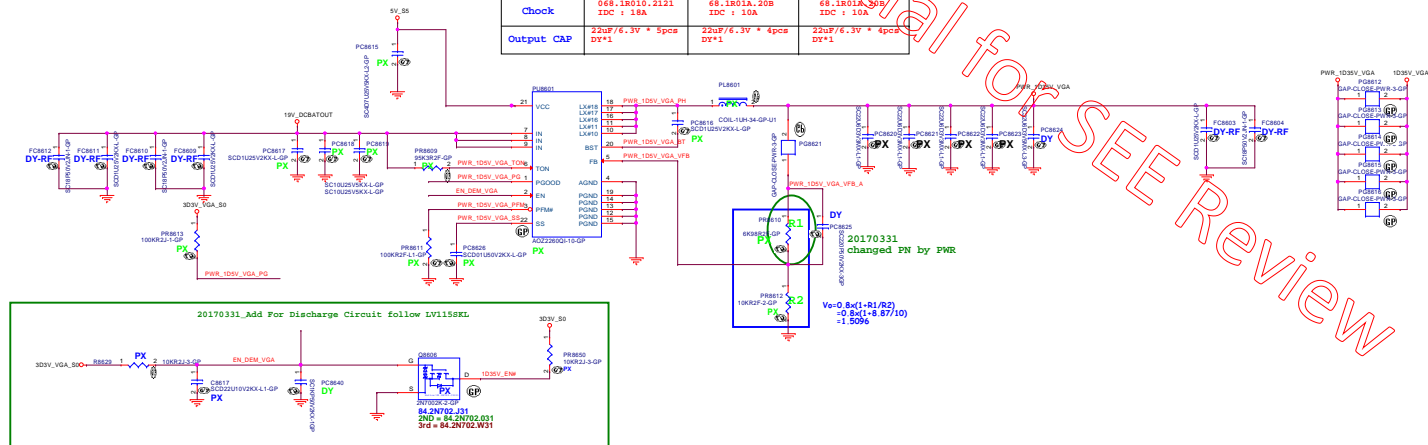
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20151106 need Add MOS to Control 1D35V\_EN# IN SB version



EE need to confirm 20170208  
EE confirm 20170413

IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
COM	068.18010.2121	68.1801A.208	68.1801A.208
Chok	IDC : 18A	IDC : 10A	IDC : 10A
Output CAP	22uF/6.3V + 5pse DY*1	22uF/6.3V + 4pse DY*1	22uF/6.3V + 4pse DY*1



cVariant Name:

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<Variant Name>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**(RESERVED)**

Size  
A4

Document Number

Rev

**Unicorn LV530 KBL MB 1A**

Date: Friday, December 15, 2017

Sheet 87 of 105

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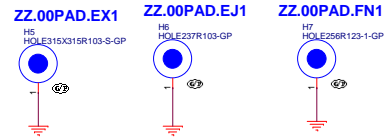
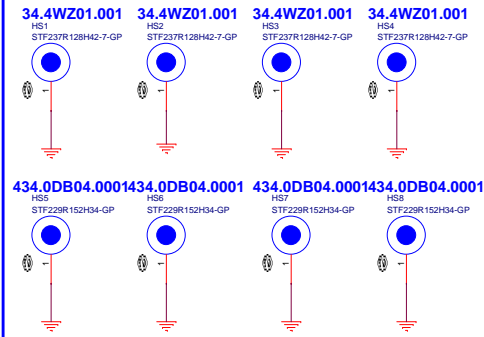
BOM1

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>RESERVED</b>			
Size A4	Document Number		Rev
<b>Unicorn LV530 KBL MB</b>		<b>GA</b>	
Date: Friday, December 15, 2017		Sheet 88	of 105

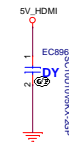
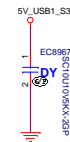
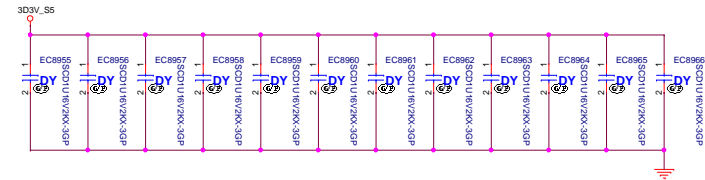
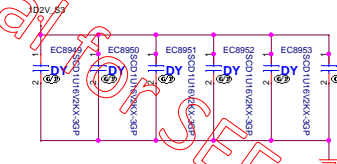
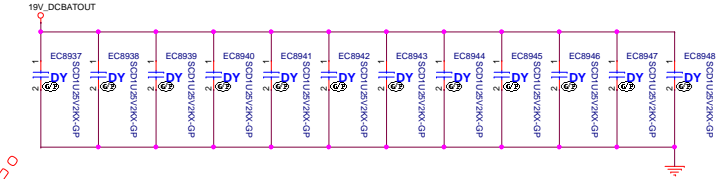
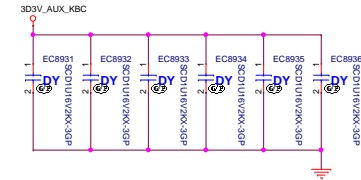
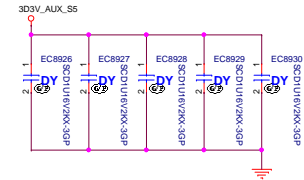
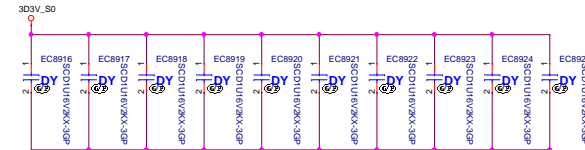
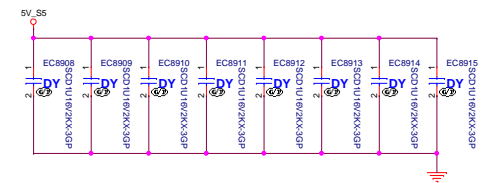
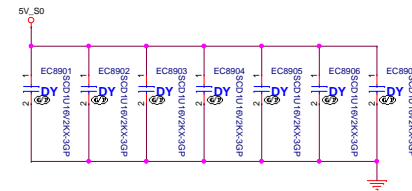
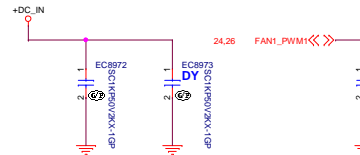
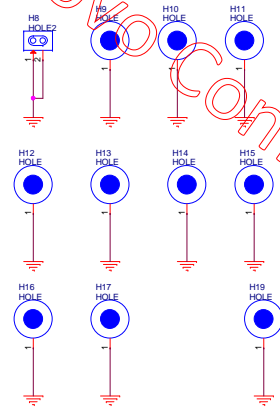
EMI Clip

EMI Clip

34.4GD01.101 will change to 434.0DB04.0001 by ME request  
Waiting for symbol



34.4LO45.001 434.07K0E.0001



BOM1

緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,  
Taipei Hsin 221, Taiwan, R.O.C.

Title  
Size Custom Document Number Rev  
Unused PARTS/EMI Capacitors  
Unicorn LV530 KBL MB54  
Date: Friday, December 15, 2017 Sheet 89 of 105

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BOM1

緯創資通

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size  
A4

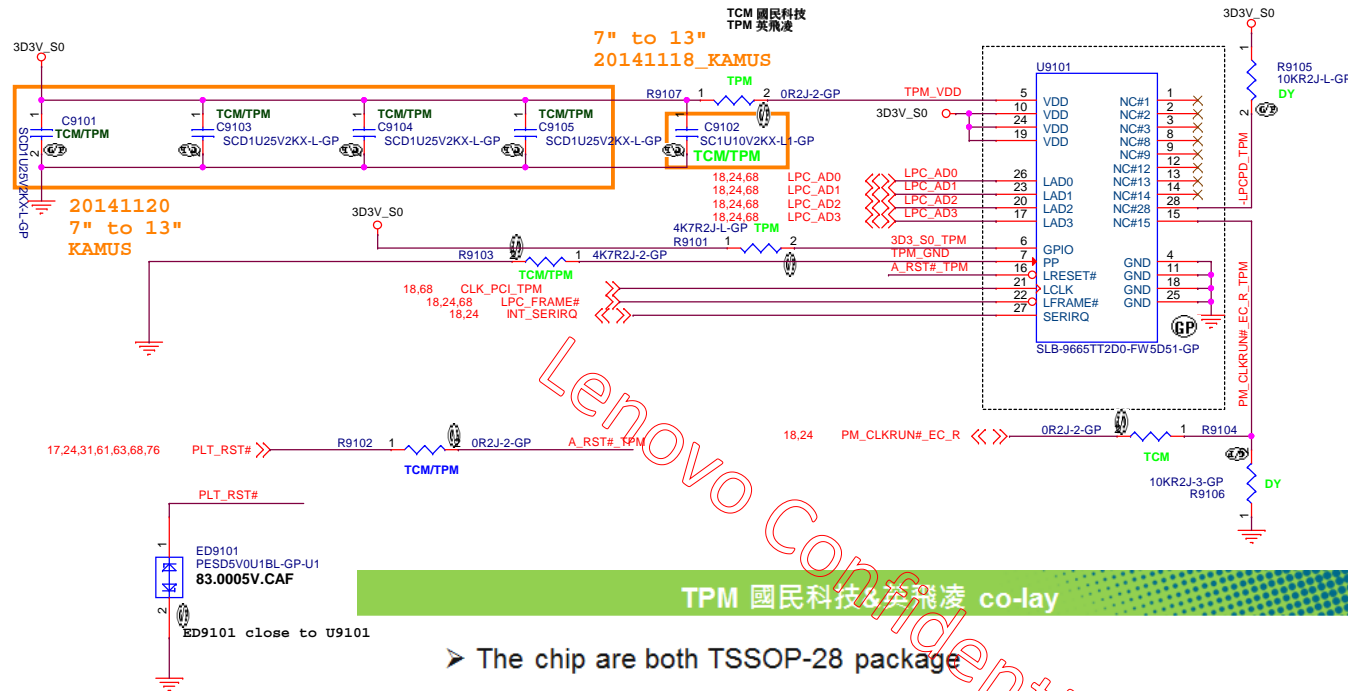
Document Number

Rev

Unicorn LV530 KBL MB 64

Date: Friday, December 15, 2017

Sheet 90 of 105



➤ The chip are both TSSOP-28 package

Pin define	國民	英飛凌	Remark	Pin define	國民	英飛凌	Remark
1	NC	NC		15	CLKRUN#	NC	0ohm
2	NC	NC		16	LRESET#	LRESET#	
3	NC	NC		17	LAD3	LAD3	
4	GND	GND		18	GND	GND	
5	NC	VDD	0ohm	19	VDD	VDD	
6	NC	GPIO	0ohm	20	LAD2	LAD2	
7	NC	PP	0ohm	21	LCLK	LCLK	33ohm for 國民
8	NC	NC		22	LFRAME#	LFRAME#	
9	NC	NC		23	LAD1	LAD1	
10	VDD	VDD		24	VDD	VDD	
11	GND	GND		25	GND	GND	
12	NC	NC		26	LAD0	LAD0	
13	NC	NC		27	SIRQ	SERIRQ	
14	NC	NC		28	LPCPD#	NC	0ohm

Czrrizo/Carrizo-Lite + Exo Pro

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title 091\_TPM

Size A3 Document Number

Date: Friday, December 15, 2017

Rev 13A

Unicorn LV530 KBL MB13A

Sheet 91 of 105

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(RESERVED)		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 92 of 105



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BOM1

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Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size  
A4

Document Number

Rev

Unicorn LV530 KBL MB 1A

Date: Friday, December 15, 2017

Sheet 93 of 105

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BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
Size	Document Number		Rev
A4	Unicorn LV530 KBL MB		1A
Date: Friday, December 15, 2017		Sheet 94 of	105

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 95 of 105

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
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A4	Unicorn LV530 KBL MB	1A
Date: Friday, December 15, 2017		Sheet 96 of 105

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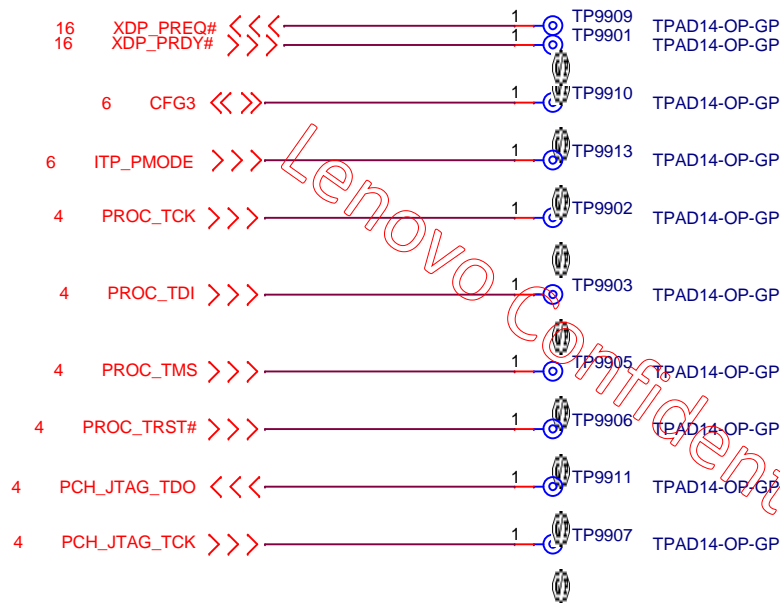
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Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 97 of 105

Lenovo Confidential for SEE Review

( Blank )

<Variant Name>

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Title			
<b>RESERVED</b>			
Size	Document Number		Rev
A4	<b>Unicorn LV530 KBL MB</b>		<b>1A</b>
Date: Friday, December 15, 2017		Sheet 98	of 105



<Variant Name>

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Title					
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Size	Document Number				Rev
A4	<b>Unicorn_LV530_KBL_MB14</b>				<b>SA</b>
Date: Friday, December 15, 2017		Sheet 99		of 105	

Lenovo Confidential for SEE Review

<Variant Name>

緯創資通

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**TABLE OF CONTENT**

Size A4	Document Number <b>Unicorn LV530 KBL MB 64</b>	Rev <b>1A</b>
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Size  
A4

Document Number

Rev

**Unicorn LV530 KBL MB 1A**

Date: Friday, December 15, 2017

Sheet 101 of 105

Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

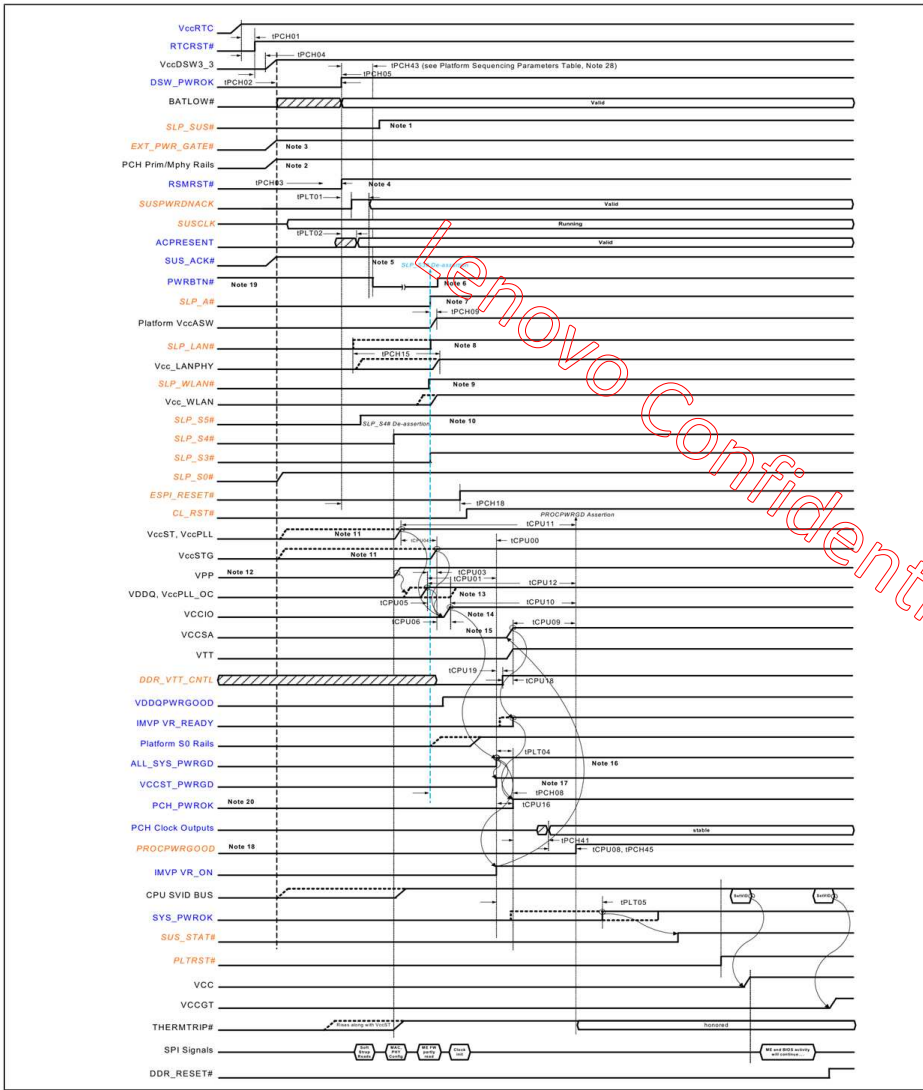


Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 2 of 2)

Notes:

1. SLP\_SUS# is ignored in Non-DSx systems
2. Refer Rail-to-Rail Power Sequencing Requirement section for details on PCH prime rail-to-rail power and power down dependencies
3. EXT\_PWR\_GATE# has been de-featured. This pin, in native mode, will never be driven low
4. For a non-DeepSx system DSW\_PWROK and RSMRST# go high at the same time (connected on board)
5. For a non-DeepSx system SUS\_ACK# will rise with prime voltage rail powering the VCCPGPPA power pin due to weak internal pull-up.
6. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
7. On first exit from G3, SLP\_A# de-asserts with SLP\_S3# de-assertion
8. High for WoL=1, Low for WoL=0. SLP\_LAN# may rise before, but no later than SLP\_A#
9. On first exit from G3, SLP\_WLAN# de-asserts with SLP\_S3# de-assertion
10. Delay between SLP\_S5#, SLP\_S4#, and SLP\_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP\_S3#, SLP\_S4#, and SLP\_S5# is not guaranteed
11. VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 42, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.
12. Only required with LPDDR3 and DDR4 memory configurations
13. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP\_S3# de-assertion due to VR ramp timing and configuration
14. VCCIO, VCCSA must ramp after VccST, VccSTG, and VDDQ have completed their ramps. If VCCSTG and VCCIO supplies are merged together as a single supply, VCCSA must ramp after VccST, VccSTG/VCCIO, and VDDQ have completed their ramps
15. IMVP\_VR\_ON is recommended to be triggered by ALL\_SYS\_PWRGD in order to help minimize boot latency.
16. ALL\_SYS\_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
17. VCCST\_PWRGD can assert before or equal to PCH\_PWROK, but must never lag it. It is recommended that both VCCST\_PWRGD and PCH\_PWROK include ALL\_SYS\_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time
18. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.
19. When "Power Button" is the trigger for wake or sleep event for the system
20. The Platform should ensure that PCH\_PWROK does not glitch when RSMRST# is de-asserted

Additional Notes:

- The state of the SLP\_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.
- SUSPWRDNACK
    - Platform not supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted OR System state is S3. Else, EC has an option to do whatever it wants with the SUS Rails
    - Platform supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted OR System state is S3 OR SLP\_A# is de-asserted OR it is the first 200ms after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails
  - Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

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**POWER BLOCK DIAGRAM**

Size  
A4

Document Number

**Unicorn LV530 KBL MB GA**

Rev

Date: Friday, December 15, 2017

Sheet 103 of 105

Lenovo Confidential for SEE Review

<Variant Name>

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**SMBUS BLOCK DIAGRAM**

Size  
A4

Document Number

**Unicorn LV530 KBL MB GA**

Rev

Date: Friday, December 15, 2017

Sheet 104 of 105

Lenovo Confidential for SEE Review

<Variant Name>

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Size <div>A4</div>	Document Number <div>Unicorn LV530 KBL MB 6A</div>	Rev <div>1A</div>
Date <div>Friday, December 15, 2017</div>		Sheet <div>105</div> of <div>105</div>